Service Guide

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For Safety and Regulatory information, see the pages at the end of the book.

Agilent Technologies 16910/11A Logic Analyzers

The Agilent 16910/11A Logic Analyzers—At a Glance

The Agilent Technologies 16910A and 16911A are logic analyzer modules for the Agilent Technologies 16900-series logic analysis system. The 16910/11A offers high performance measurement capability.

Features

Some of the main features of the 16910/11A are as follows:

- 98 data channels (16910A)
- 64 data channels (16911A)
- 4 clock/data channels
- 256 K to 64 M memory depth per channel (depends upon option chosen)
- 500 Mb/s maximum state data rate (with Option 500)
- 1 GHz, 128 M deep timing analysis on half channels
- “Eye Finder” feature
- 4 GHz timing zoom with 64 k memory depth
- Expandable to 340 channels (16911A) or 510 channels (16910A) on a single clock

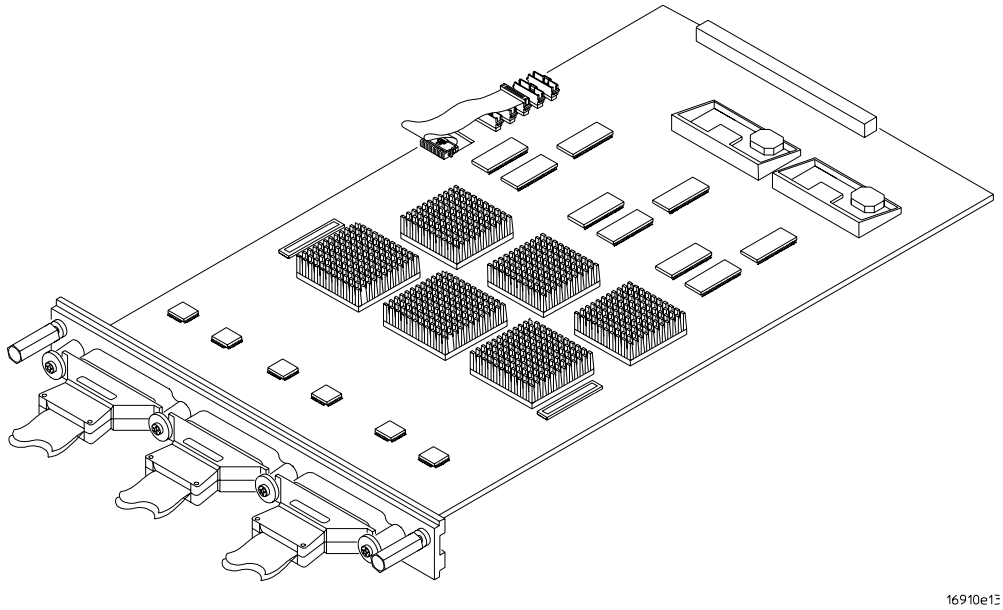
Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16910/11A state and timing analyzer module.

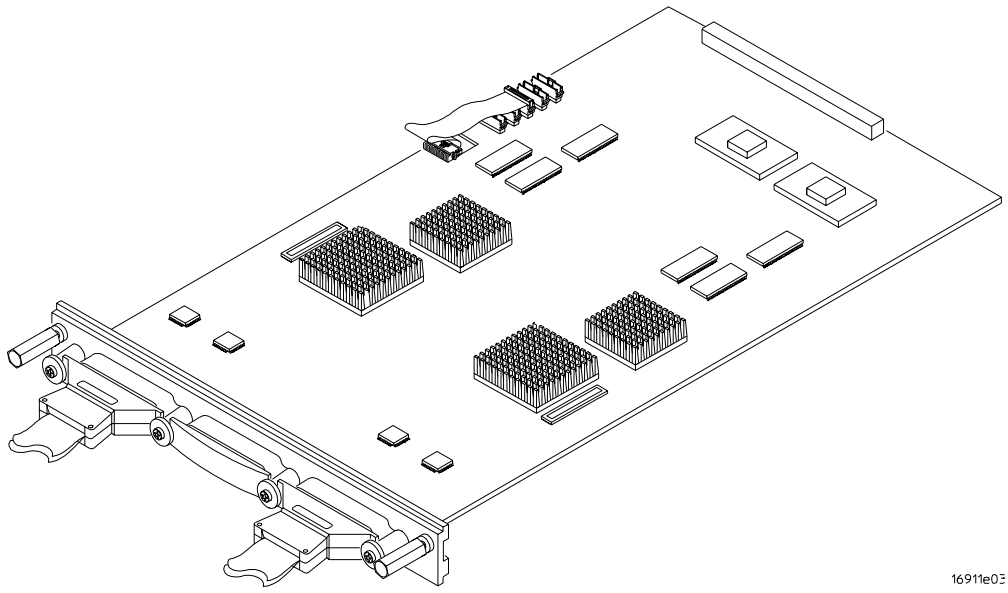
The modules can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

Application

This service guide applies to a 16910A or 16911A module installed in the 16900-series logic analysis system mainframes.



The 16910A Logic Analyzer



The 16911A Logic Analyzer

In This Book

This book is the service guide for the 16910A and 16911A logic analyzer modules.

This service guide has eight chapters.

Chapter 1, “General Information,” beginning on page 9 contains information about the module and includes accessories for the module, specifications and characteristics of the module, and a list of the equipment required for servicing the module.

Chapter 2, “Preparing for Use,” beginning on page 15 tells how to inspect and prepare the module for use.

Chapter 3, “Testing Logic Analyzer Performance,” beginning on page 19 gives instructions on how to test the performance of the module.

Chapter 4, “Calibrating,” beginning on page 61 contains calibration instructions for the module (if required).

Chapter 5, “Troubleshooting,” beginning on page 63 contains flowcharts for troubleshooting the module and an explanations of the self-tests.

Chapter 6, “Replacing Assemblies,” beginning on page 83 explains how to replace the module and assemblies of the module and how to return them to Agilent Technologies.

Chapter 7, “Replaceable Parts,” beginning on page 89 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8, “Theory of Operation,” beginning on page 97 explains how the logic analyzer works.

Contents

Contents

1

General Information

This chapter lists the accessories, some of the specifications and characteristics, and the recommended test equipment.

Accessories

One or more of the following accessories, sold separately, are required to operate the 16910/11A logic analyzers.

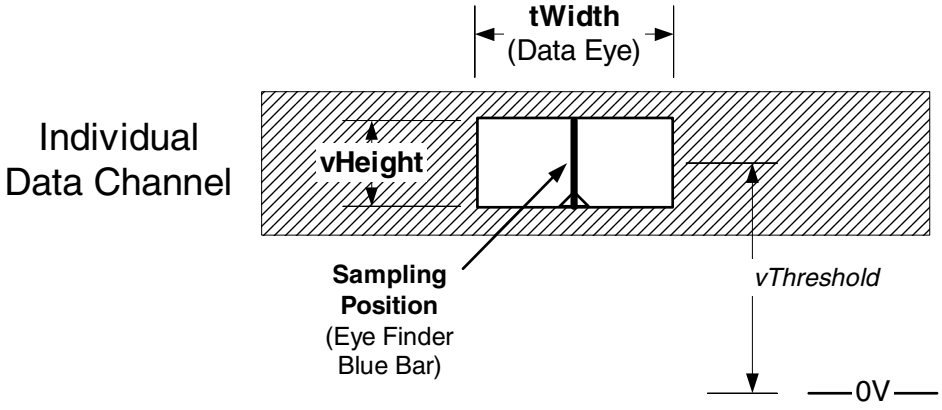
Accessories	Agilent Part Number
Flying Lead Probe Set	E5383A
17-Pin Single-Ended Soft Touch Probe	E5396A
34-Pin Single-Ended Soft Touch Probe	E5394A
100-Pin Single-Ended Probe (Samtec)	E5385A
38-Pin Single-Ended Probe (MICTOR)	E5346A
Single-Ended Low Voltage Probe (MICTOR)	E5339A
Single-Ended Probe, No Isolation Networks (MICTOR)	E5351A

Mainframe and Operating System

The 16910/11A logic analyzers require an Agilent Technologies 16900-series logic analysis system (mainframe). The 16910/11A logic analyzers (module) will work with any version of the 16900-series logic analysis system operating system.

Specifications

The specifications are the performance standards against which the product is tested.



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Specifications			
Parameter	**250 Mb/s mode**	**500 Mb/s mode**	**Notes**
Minimum master to master clock time	4 ns	2 ns	500 Mb/s mode is available only when Option 500 is installed.
tWidth (minimum)	1.5 ns	1.5 ns	Specified at probe tip. Eye width as measured by Eye Finder may be less.

Specifications verified under the following test conditions:			
Parameter	**250 Mb/s mode**	**500 Mb/s mode**	**Notes**
Vh	1.3 V		600 mVp-p
Vl	0.7 V		
vThreshold	1 V		
rise/fall times	150-180 ps		
Probe	Agilent E5383A		Flying Lead Probe

Environmental Characteristics

Probes	
Maximum Input Voltage	± 40 V, CAT I, CAT I = Category I, secondary power line isolated circuits.
Operating Environment	
Temperature	0 to 40 °C (+32 °F to 104 °F) when operating in a 16900A or 16902A mainframe. 0 to 50 °C (+32 °F to 122 °F) when operating in a 16903A mainframe.
Humidity	Up to 80% relative humidity at 40 °C (+104 °F). Reliability is enhanced when operating within the range 20% to 80% non-condensing.
Altitude	0 to 3000 m (10,000 ft).
Vibration	Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.2 g (rms).
	Operating power supplied by mainframe. Indoor use only. Pollution Degree 2.

See the 16900-series logic analyzer's online help system for a full listing of all specifications and characteristics.

Recommended Test Equipment

Recommended Test Equipment

Equipment	Critical Specifications	Recommended Agilent Model/Part	Use†
Single-ended Flying Lead Probe Set (Qty 2)	no substitute	E5383A	P, T
Ground Leads (Qty 5)	no substitute	pkg of 5 (Included with E5383A Probe Set)	T
Pulse Generator	260 MHz,1 ns pulse width, two channels, ≤ 150 ps rise time	8133A Option 003	P, T
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps (Voffset = 1V, ΔV = 600 mV). Required for 8133A opt. 003	Agilent or HP 15435A	P
Oscilloscope	≥ 1.5 GHz bandwidth, ≥ 8 GSa/s sampling rate	54845A or 54845B	P
SMA/Flying Lead Test connectors	no substitute	See "To Assemble the SMA/Flying Lead Test Connectors" on page 22	P
2 x 9 Test connectors	no substitute	See "To Assemble the 2 x 9 Test Connectors" on page 71	P
SMA Coax Cable (Qty 2)	≥ 18 GHz bandwidth	8120-4948	P

†P = Performance Tests, T = Troubleshooting

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Preparing for Use

This chapter gives you instructions for preparing the logic analyzer module for use.

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed on page 12. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given on page 12. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20°C to +35°C (+68°F to +95°F)

Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40°C to +75°C (-40°F to +167°F)
- Humidity: Up to 90% at 65°C (+149°F)
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

One or more of the accessories listed on page 10 are required to operate the 16910/11A logic analyzer module.

3 Inspect the product for physical damage.

Check the module and the supplied accessories for obvious physical or

mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To configure and install the module

Instructions for configuring and installing the module into the mainframe can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16900A-series mainframe, go to www.agilent.com and enter **16900A installation guide** in the quick search box. Then scroll down to **Manuals, Guides & Notifications** to find the *16900A-Series Logic Analysis Systems Installation Guide*.

To test the module

The logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, see the "Testing Logic Analyzer Performance" chapter on page 19. If you require a test to verify correct module operation using software self-tests, see "Do a self-test on the logic analysis system." on page 30.
- If the module does not operate correctly, see "Troubleshooting" on page 63.

To clean the module

- With the mainframe turned off and unplugged, use a cloth moistened with a mixture of mild detergent and water to clean the rear panel.
- Do not attempt to clean the module circuit board.

3

Testing Logic Analyzer Performance

This chapter tells you how to test the performance of the 16910A or 16911A logic analyzer against the specifications listed on page 11.

To ensure the 16910A or 16911A logic analyzer (also referred to as the module or the card) is operating as specified, software tests (self-tests) and a manual performance test are done. The logic analyzer is considered performance-verified if all of the software tests and the manual performance test have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

Test Strategy

This chapter describes the module being tested in an Agilent Technologies 16900A-series mainframe.

Only specified parameters are tested. Specifications are listed on page 11. The test conditions defined in this procedure ensure that the specified parameter is as good as or better than specification. No attempt is made to determine performance which is better than specification. Not all channels of the logic analyzer will be tested; rather a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

One-card Module. To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Multi-card Module. To perform a complete test on a multi-card module, perform the self-tests (page 30) with the cards connected. Then, remove the multi-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into their original multi-card module configuration, reinstall it into the mainframe and perform the self-tests again. These steps are necessary to ensure that the clocks are tested on each module.

For removal instructions see Chapter 6, "Replacing Assemblies," beginning on page 83. For installation and configuration instructions see Chapter 2, "Preparing for Use," beginning on page 15.

Test Interval

Test the performance of the module against specifications at two-year intervals.

Test Record Description

A Performance Test Record for recording the results of each procedure is located at the end of this chapter.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number.

Instrument Warm-Up

Before testing the performance of the module, warm-up the logic analyzer and the test equipment for 30 minutes.

To Assemble the SMA/Flying Lead Test Connectors

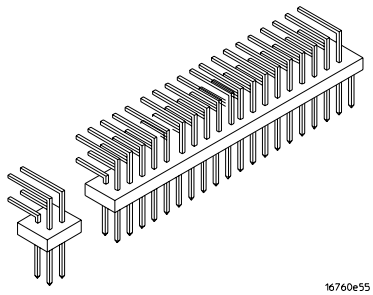
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the required test connectors.

Materials Required

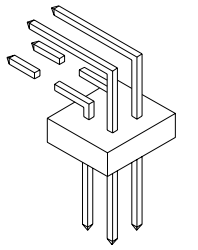
Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 6)		Johnson 142-0701-801 (see www.johnsoncomponents.com)
Pin Strip Header (Qty 1, which will be separated)	.100" X .100" Pin Strip Header, right angle, pin length .230", two rows, .120" solder tails, 2 X 40 contacts	3M 2380-5121TN or similar 2- row with 0.1" pin spacing
SMA 50 ohm terminators (Qty 1)	Minimum bandwidth 2 GHz	Johnson 142-0801-866 50 ohm Dummy Load Plug
SMA m-m adapter (Qty 3)		Johnson 142-0901-811 SMA Plug to Plug or similar

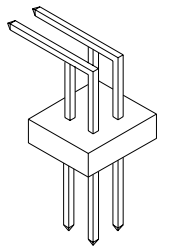
1 Prepare the pin strip header:

a Cut or cleanly break a 2 x 2 section from the pin strip.

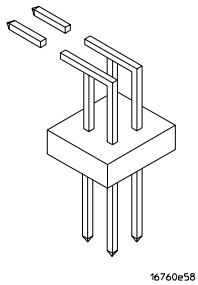


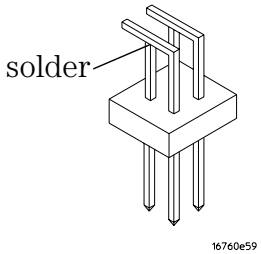
b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.





c Trim about 2.5 mm from the outer leads.



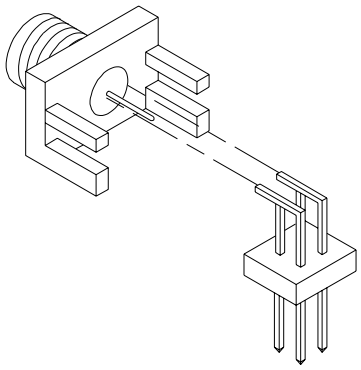


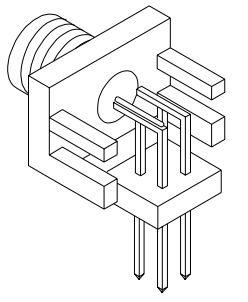
d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.

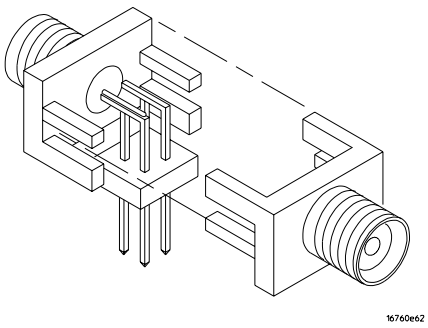


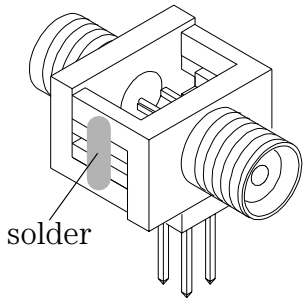


3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.





c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

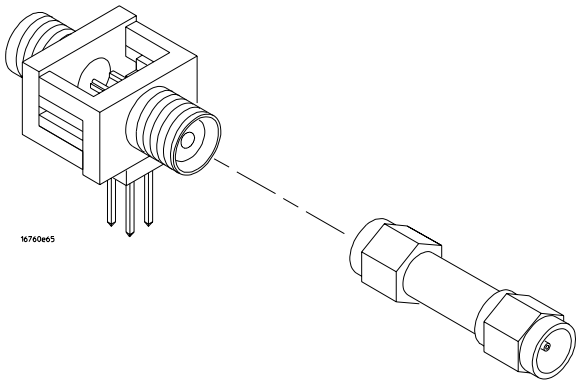
a Ensure that the following four points have continuity between them: The two pins on the left side of the pin strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

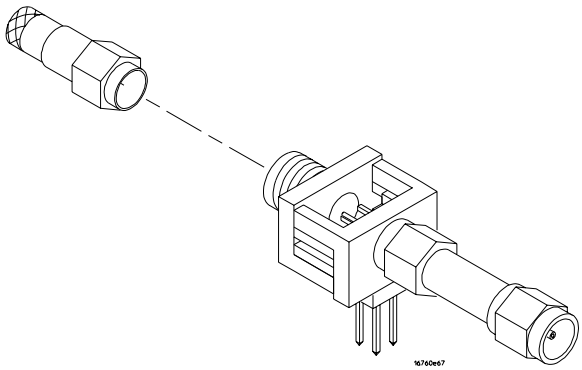
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

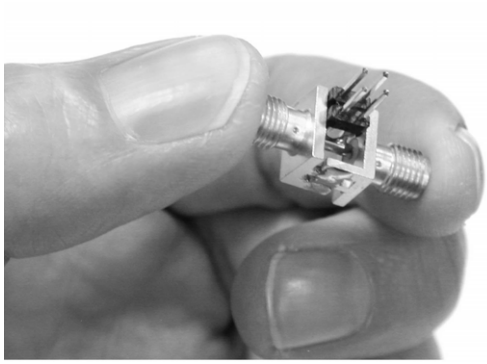
a Attach an SMA m-m adapter to one end of each of the three SMA/Flying Lead test connectors.

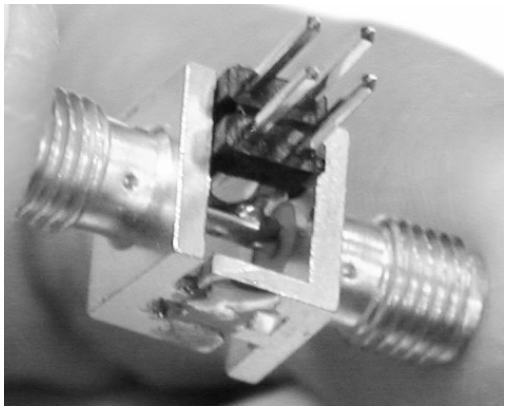


b Attach a 50 ohm terminator to the other end of just one of the SMA/ Flying Lead test connectors.



c The finished test connector is shown in the pictures below.





To Test the Minimum Master to Master Clock Time and Minimum Eye Width

The specifications for the 16910/11A logic analyzer define a minimum master to master clock time and a minimum data eye width at which data can be acquired. This test verifies that the logic analyzer meets these specifications.

Eye Finder is used to adjust the sampling position on every tested channel. Eye Finder must be used to achieve minimum data eye width performance.

First, the logic analyzer will be tested in the 250 Mb/s state mode. Then it will be tested in the 500 Mb/s state mode.

In the 250 Mb/s state mode each pod will be tested with its respective clock.

The 500 Mb/s mode has only one clock (Clk1). All tests in the 500 Mb/s mode will use clock Clk1.

A sample of four channels on each pod will be tested, one pod at a time, in both 250 Mb/s state mode and 500 Mb/s state mode.

The logic analyzer will be configured to acquire data on both edges of the clock, so the test frequency is set to half of the acquisition speed.

Equipment Required

The following equipment is required for the performance test procedure.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	≥ 260 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Agilent or HP 8133A option 003
150 ps Transition Time Converter (Qty 3)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset = 1V, ΔV = 500 mV.) Required for 8133A opt. 003.	Agilent or HP 15435A
Oscilloscope	bandwidth ≥ 1.5 GHz, sampling rate ≥ 8 GSa/s	Agilent or HP 54845A/B or similar
SMA Coax Cable (Qty 2)	> 18 GHz bandwidth	Agilent or HP 8120-4948
Flying Lead Probe Set with 5 ground leads (Qty 2)	no substitute	Agilent or HP E5383A
Male BNC to Female SMA adapters (Qty 2)		Cambridge Products CP-AD507 (see www.cambridgeproducts.com)
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 3)	no substitute	See "To Assemble the SMA/Flying Lead Test Connectors" on page 22

Prepare the Logic Analysis System for Testing

1. Record the 16910A or 16911A logic analyzer's model and serial number in the Performance Test Record (see page 60). Record your work order number (if applicable) and today's date.
2. Record the test equipment information in the "Test Equipment Used" section of the Performance Test Record.
3. Turn on the logic analysis system.
   a. Connect the keyboard and monitor to the rear panel of the logic analysis mainframe (16900A only).
   b. Connect the mouse to the rear panel of the mainframe.
   c. Plug in the power cord to the power connector on the rear panel of the mainframe.
   d. Turn on the main power switch on the mainframe front panel.

      While the logic analysis system is booting, observe the boot dialog for the following:

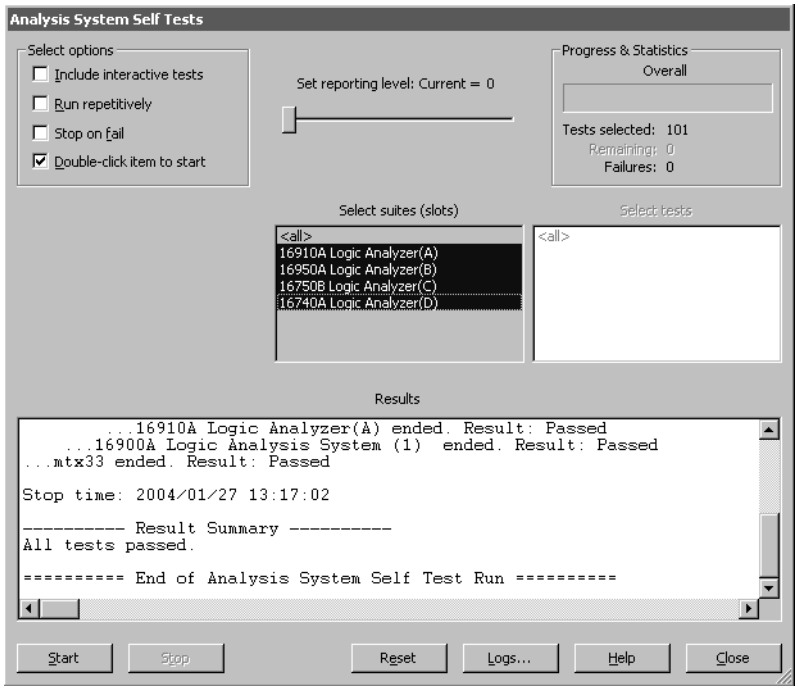
      - ensure all of the installed memory is recognized
      - any error messages
      - interrupt of the boot process with or without error message
4. During initialization, check for any failures.

   If an error or an interrupt occurs, refer to the *Agilent Technologies 16900A-series Logic Analysis System Service Guide* for troubleshooting information.

Perform System Self-Tests

5 Do a self-test on the logic analysis system.

a When the logic analysis system has finished booting, the Waveform window appears. Select Help→Self-Test... from the main menu. The Analysis System Self Tests window will appear.



b In the Select Suite(s) list, select <all>. This will cause <all> to be selected in the Select Test(s) list.

c Select Start. This will perform a complete system self-test.

The progress of the self tests is displayed in the Progress & Statistics area of the window.

d When the self-tests are complete, check the Results window to ensure that the Result Summary says that all tests passed. If all tests did not pass, refer to "Troubleshooting" on page 63.

e Select the Close button to close the Analysis System Self Tests window.

f If all module self-tests pass, then record "PASS" in the "Logic Analysis System Self-Tests" section of the Performance Test Record (page 60).

Set Up the Test Equipment

1 Turn on the required test equipment. Let all of the test equipment and the logic analyzer warm up for 30 minutes before beginning any test.

2 Set up the pulse generator according to the following table.

a Set the frequency of the pulse generator. In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 125 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

For example, if you are using an 8133A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 125 MHz plus 2% (127.5 MHz).

b Set the rest of the pulse generator parameters to the values shown in the following table.

Pulse Generator Setup

Timebase	Pulse Channel 2	Trigger	Pulse Channel 1
Mode: Int	Mode: Pulse ÷ 1	Disable (LED on)	Mode: Square
Freq: was set in previous step.	Delay: (not available in pulse mode)		Delay: 0 ps
	Width: Initially set to 1.5 ns. Change later (on page 39).		Width: (not available in square mode)
	Ampl: 0.6 V		Ampl: 0.6 V
	Offs: 1.0 V		Offs: 1.0 V
	Output: Enable (LED off)		Output: Enable (LED off)
	Comp: Normal (LED off)		Comp: Normal (LED off)
	Limit: Off (LED off)		Limit: Off (LED off)
	$\overline{\text{Output}}$: Enable (LED off)		$\overline{\text{Output}}$: Enable (LED off)

3 Set up the oscilloscope.

a Set up the oscilloscope according to the following tables.

Oscilloscope Setup

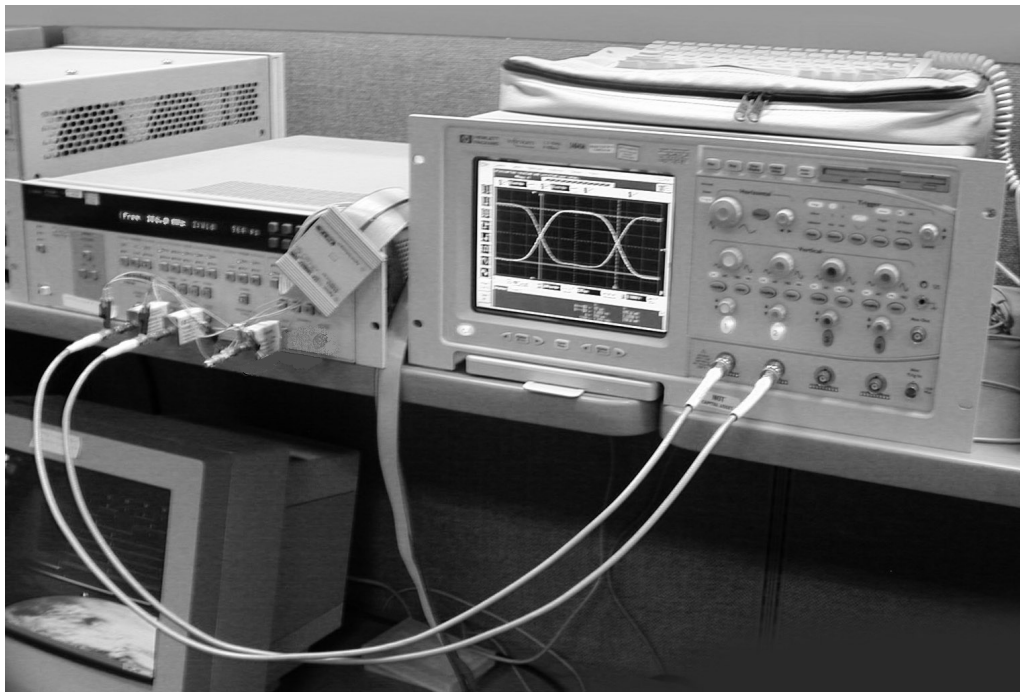
Setup: Channel 1	Setup: Ch. 1 Probe	Setup: Channel 2	Setup: Ch. 2 Probe
On	Attenuation: 1.00:1	On	Attenuation: 1.00:1
Scale: 100 mV/div	Units: Volts	Scale: 100 mV/div	Units: Volts
Offset: 1 V	Attenuation Units: Ratio	Offset: 1 V	Attenuation Units: Ratio
Coupling: DC	External Gain: (n/a)	Coupling: DC	External Gain: (n/a)
Input: 50 ohm	Skew: (Set later. See page 37)	Input: 50 ohm	Skew: 0.0 seconds
	External Offset: (n/a)		External Offset: (n/a)

Setup: Channel 3	Setup: Channel 4
Off	Off

Setup: Horizontal	Setup: Trigger	Setup: Acquisition	Setup: Display
Scale: 2 ns	Mode: Edge	Sampling Mode: Equiv. Time	Waveforms: Connect dots
Position: 725 ps	Source: Channel 1	Memory Depth: Automatic	Persistence: Minimum
Reference: Center	Level: 1.00 V	Averaging: Enabled	Grid: On (and set intensity)
Delayed: not selected	Edge: Rising Edge	# of Averages: 4	Backlight Saver: as preferred
	Sweep: Auto		

Measure: Markers
Mode: Manual placement
All else: (n/a)

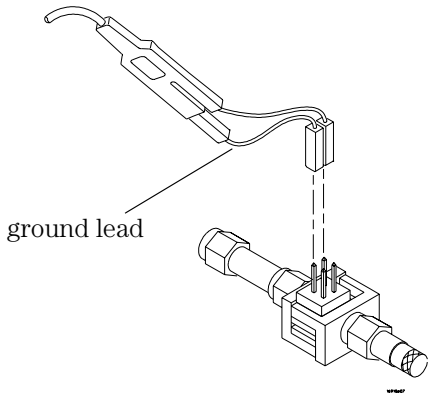
Connect the Test Equipment



Connect the 16910/11A Logic Analyzer Pod to the 8133A Pulse Generator

1. Connect a Transition Time Converter (if required—see page 28) to each of the four outputs of the 8133A pulse generator except Channel 1 $\overline{\text{OUTPUT}}$.
2. Connect the SMA/Flying Lead test connector (see "To Assemble the SMA/Flying Lead Test Connectors" on page 22) *with* the 50 ohm terminator to the Transition Time Converter at the 8133A pulse generator Channel 1 OUTPUT. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connector directly to the pulse generator output.)
3. Connect the two SMA/Flying Lead test connectors *without* 50 ohm terminators to the Transition Time Converters at the 8133A pulse generator Channel 2 OUTPUT and Channel 2 $\overline{\text{OUTPUT}}$. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)
4. Connect an E5383A Flying Lead Probe Set to Pod 1 of the 16910/11A logic analyzer.

5 Connect the E5383A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the 8133A pulse generator's Channel 1 OUTPUT.



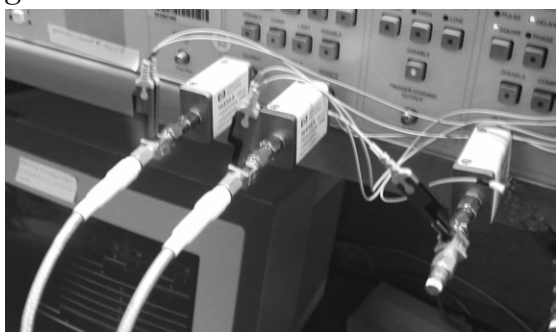
NOTE: For each Flying Lead Probe connection, be sure to use a black ground lead (five are supplied with the E5383A Flying Lead Probe Set) and orient the leads so that the ground leads are connected to the SMA/Flying Lead connector's ground pins!

If you don't have the ground leads, you can push the probe body's ground socket directly onto a ground pin on the SMA/Flying Lead test connector. However, this will bend and could break pins on the SMA/Flying Lead test connector because the probe body spacing is greater than the SMA/Flying Lead test connector pin spacing. It is better to use the black ground leads.

In any case, the probe ground must be connected for each channel.

6 Connect the E5383A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 $\overline{\text{OUTPUT}}$.

7 Connect the E5383A Flying Lead Probe Set's bits 6 and 14 to the SMA/ Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 OUTPUT.



Connect the 8133A Pulse Generator Output to the 54845A Oscilloscope

8 Attach Male BNC to Female SMA adapters to Channels 1 and 2 on the 54845A oscilloscope.

9 Attach one end of an SMA cable to the Male BNC to Female SMA adapter on Channel 1 of the oscilloscope.

10 Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 OUTPUT of the 8133A pulse generator.

11 Attach one end of the other SMA cable to the Male BNC to Female SMA adapter on Channel 2 of the oscilloscope.

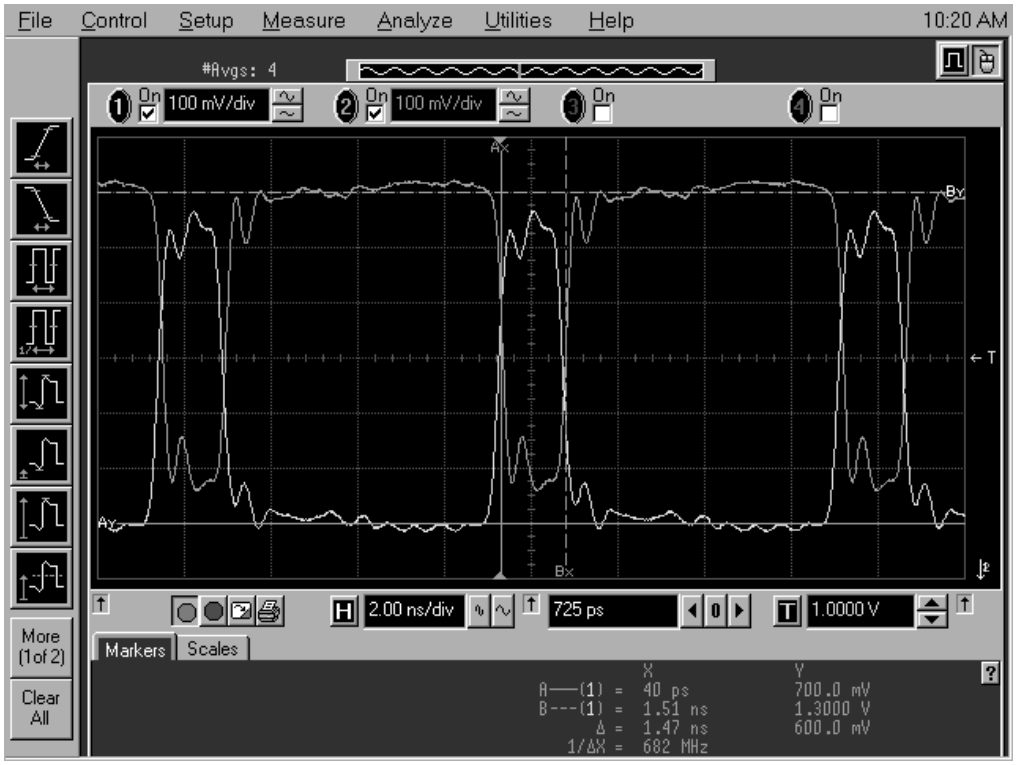
12 Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 $\overline{\text{OUTPUT}}$ of the 8133A pulse generator.

Verify and adjust 8133A pulse generator DC offset

1 On the 54845A oscilloscope, select Measure from the menu bar at the top of the display.

2 Select Markers...

3 In the Markers Setup window set marker “Ay” to 0.7 V, and set marker “By” to 1.3 V.

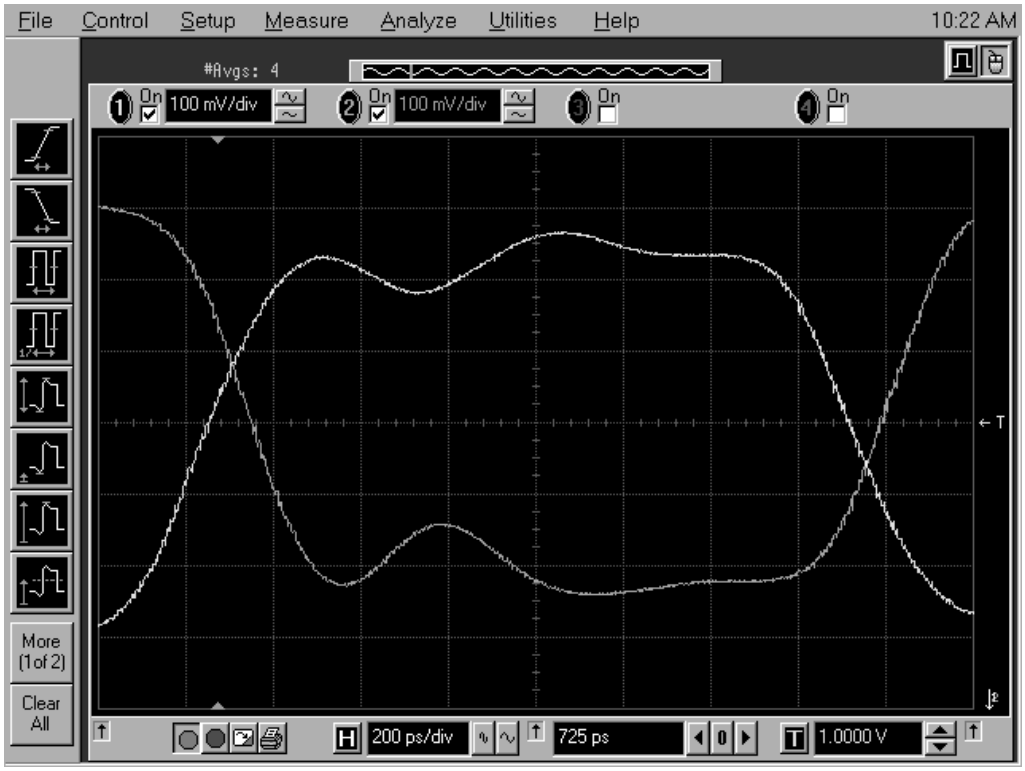


4 Observe the waveforms on the oscilloscope display. If they are not centered within the “Ay” and “By” markers, adjust the 8133A pulse generator’s Channel 1 OFFSET until the waveforms are centered as close as possible. (The resolution of the 8133A OFFSET setting is 10 mV.)

Deskew the oscilloscope

This procedure neutralizes any skew in the oscilloscope's waveform display.

1 On the 54845A oscilloscope, change the Horizontal scale to 200 ps/div. You can do this using the large knob in the Horizontal setup section of the front panel.



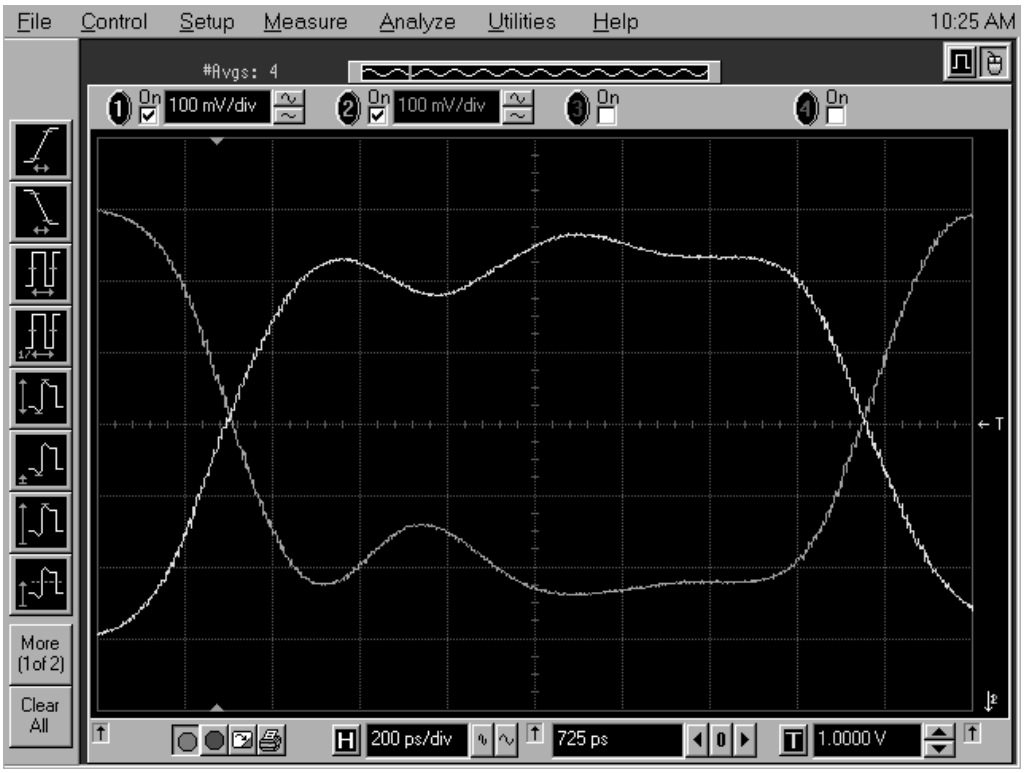
2 Select Setup from the menu bar at the top of the display.

3 Select Channel 1.

4 Select Probes.

5 Click Skew </> to deskew Channel 1 and Channel 2 signals so that both channels cross the 54845A horizontal center line at the same time, at both ends of the eye (both crossings of the horizontal center line). The horizontal center of the graticule line is at 1 volt because the vertical offset

was set to 1 volt in the oscilloscope setup described on page 32.



6 Select **Close** in the Probe Setup window.

7 Select **Close** in the Channel Setup window.

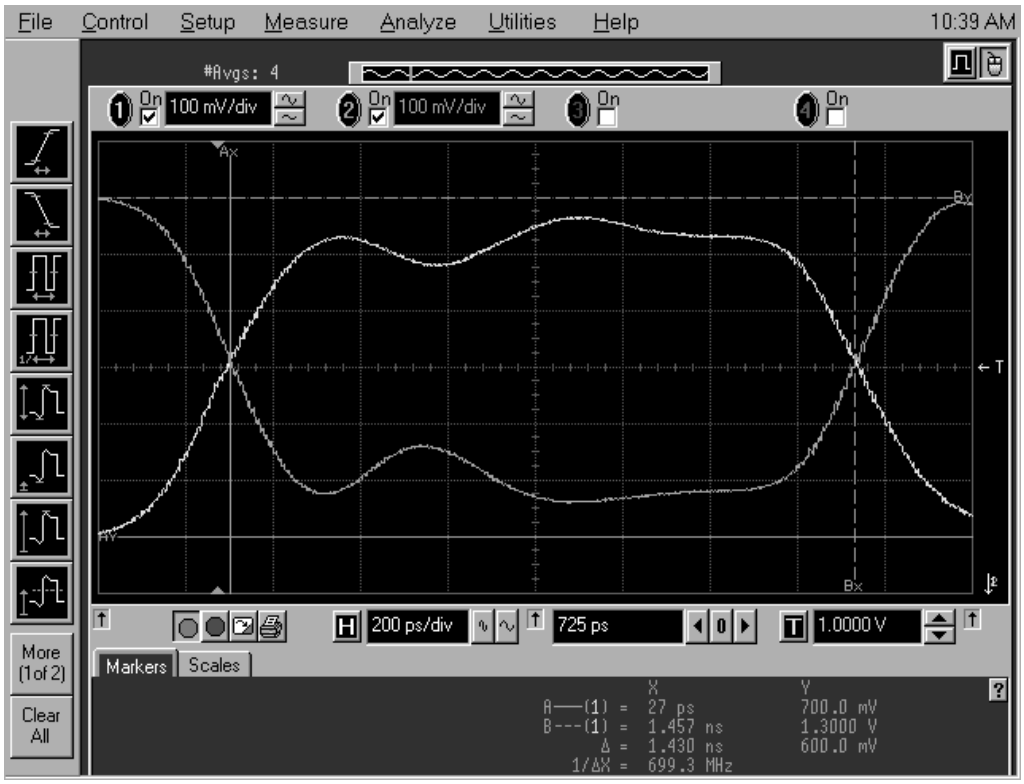
Set the 8133A pulse width

1. On the 8133A pulse generator, set the Channel 2 pulse width to 1.5 ns.
2. Observe the 54845A oscilloscope display. Change the Channel 2 pulse width of the 8133A pulse generator so that the pulse width measured at 1 volt on the oscilloscope is equal to 1.5 ns minus the measurement uncertainty and display resolution of the oscilloscope, further reduced by 35 ps for test margin.

   If you are using the 54845A/B oscilloscope, the measurement uncertainty is ±((0.007% * Δt) + (full scale/2x memory depth) + 30 ps) = ±30.10 ps. Add 5 ps for display resolution. Add 35 ps test margin.

   1.5 ns - 30.10 ps - 5 ps - 35 ps = 1.43 ns. Set the pulse width as measured on the 54845A/B oscilloscope to 1.43 ns.

NOTE: On the oscilloscope move the Ax and Bx markers to the crossing points of the pulse and the horizontal center line. Read the pulse width at the bottom of the screen. It is displayed as "Δ=".



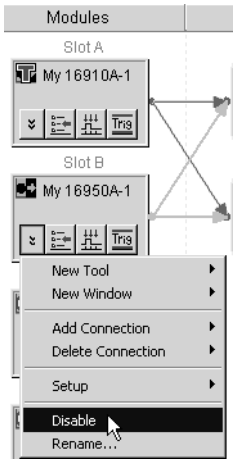
Configure the Logic Analysis System

1 Exit the logic analysis application (from the main menu, choose File→Exit) and then restart the application. This puts the logic analysis system into its initial state.

2 Disable all logic analyzers other than the analyzer under test.

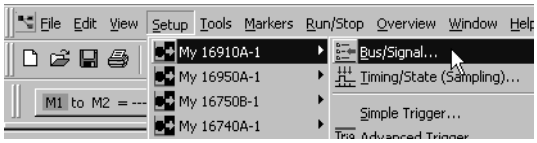
a Select the Overview tab at the bottom of the main window.

b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.



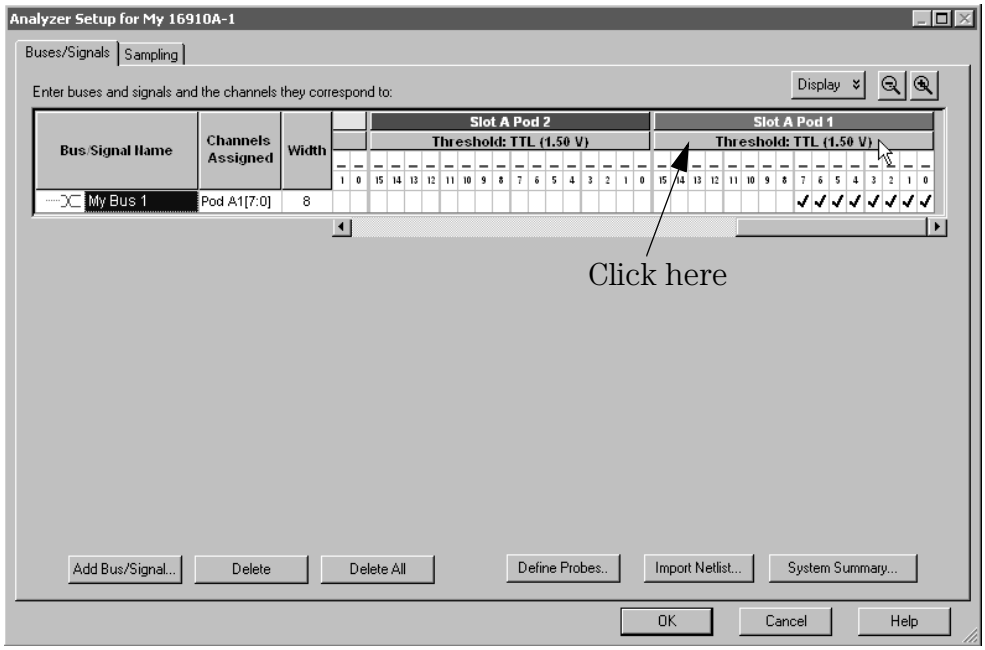
3 Set up the bus and signals.

a From the Logic Analysis System main menu, select Setup→My 1691xA→Bus/Signal....

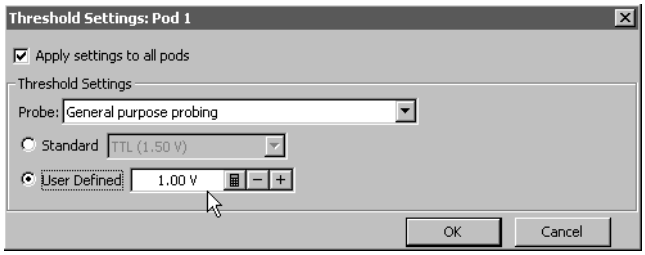


b In the Analyzer Setup window, choose the Threshold button for Pod 1.

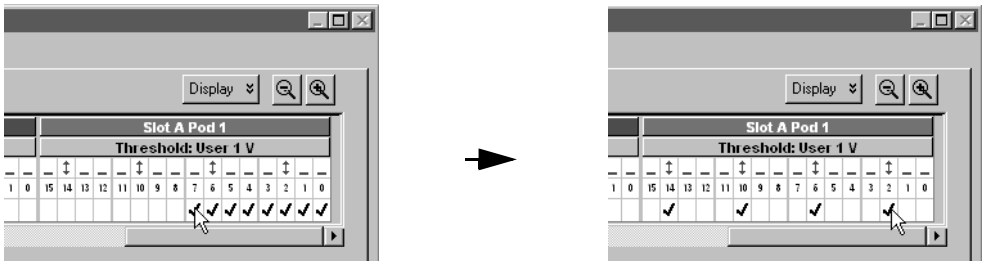
The Threshold Settings window will appear.



c Set the threshold value for Pod 1 of the 16910/11A logic analyzer to 1 V and select OK.



d The activity indicators will now show activity on the channels that are connected to the pulse generator.

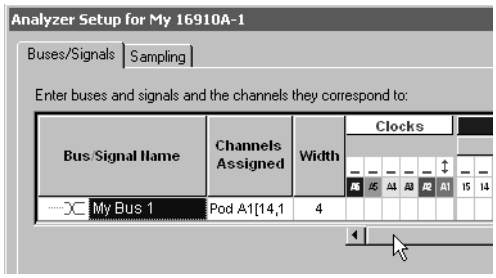


e Un-assign all channels. Hint: you can do this quickly by clicking on the left-most check mark and dragging to the right across all of the other check marks. If you have a model 16902A logic analysis system

mainframe you can touch the touchscreen and drag across with your finger.

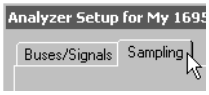
f Click (or touch) to select channels 2, 6, 10 and 14 as shown.

g Drag the scroll bar all the way to the left and ensure that the activity indicator shows activity on clock 1.

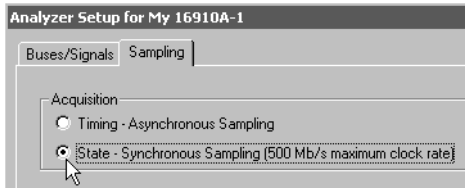


4 Set the sampling mode.

a Select the Sampling tab of the Analyzer Setup window.

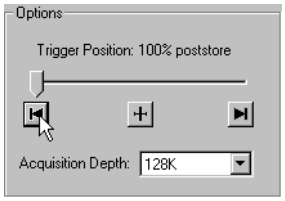


b Select State Mode.

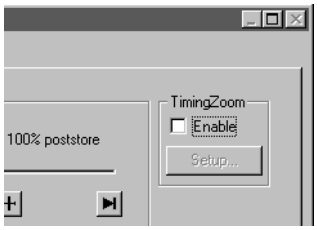


c Set the Trigger Position to 100% Poststore.

d Set the Acquisition Depth to 128K.



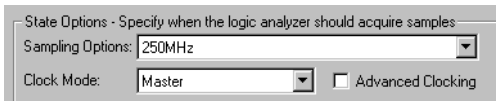
e Clear the Timing Zoom check box to turn Timing Zoom off.



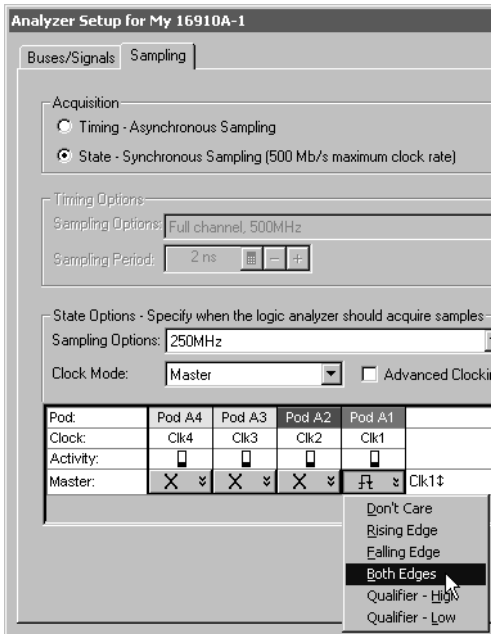
f Ensure that the sampling speed is set to **250 MHz** in the Sampling Options box.

NOTE: If option 500 is not installed on the 16910/11A module, then 250 MHz will be the only speed available.

g Ensure that the Clock Mode is set to **Master**.

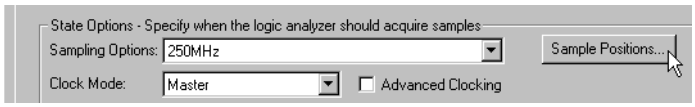


h Set the clock mode to **Both Edges**.

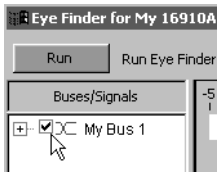


Adjust the sample positions using Eye Finder

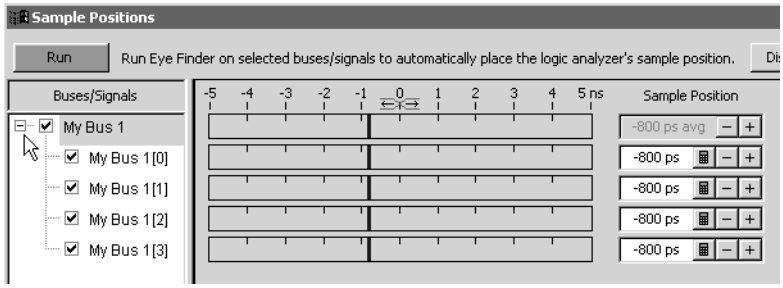
1 Select the Sample Positions button. The Eye Finder window will appear.



2 In the "Buses/Signals" section of the Eye Finder window, ensure that the check box next to "My Bus 1" is checked.



3 Select the plus sign to expand bus "My Bus 1".



Align the blue bars vertically

The first time you run Eye Finder, the blue bars will already be vertically aligned (as shown above). In this case you can skip to the next section ("Run Eye Finder").

After running Eye Finder, the blue bars will not be vertically aligned because an independent sample position will be determined for each channel.

4 If the blue bars in the Eye Finder display are not vertically aligned, grab the right-most blue bar in the "My Bus 1" row with the mouse pointer and move it all the way to the left. Release the mouse button. This will vertically align all of the blue bars.

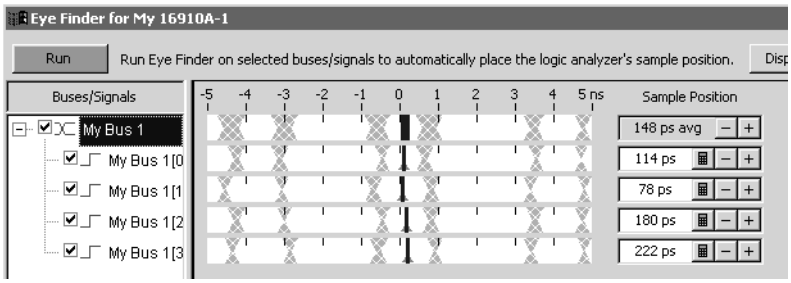
5 Using the mouse pointer, grab the top blue bar for "My Bus 1" and move it to the recommended starting position of 300 ps. All of the blue bars below will follow.

Run Eye Finder

6 Select the Run button in the Eye Finder window.

7 Ensure that an eye appears for each bit near the recommended starting position. Depending on your test setup, the eye position may vary. Any skew between channel 1 and channel 2 of your pulse generator will cause the eye position to shift to the left or right in the Eye Finder display. A shift of up to 0.5 ns should be considered normal.

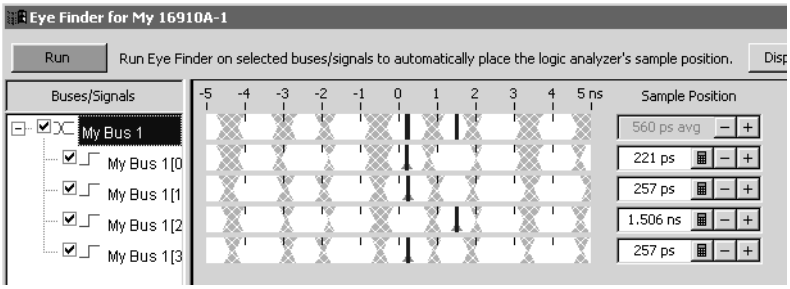
The important point is that your Eye Finder display should look similar to the picture below (although it may be shifted left or right), and Eye Finder must be able to place the blue bars in the narrow eye. (The example below shows Eye Finder in the 250 Mb/s mode.)



To re-align a stray channel

If the blue bar for a particular bit does not appear in its eye near the recommended starting position, then do the following steps to realign the sampling position of the stray channel.

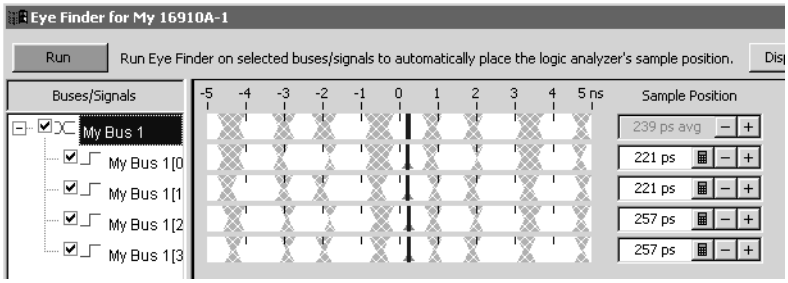
In the following example, the sampling position of one channel (My Bus 1 [2]) must be realigned with the sampling position of the other channels. (The following example shows the analyzer in the optional 500 Mb/s mode. That is why the eyes are closer together.)



8 Using the mouse, drag the sample position (blue bar) of the stray channel (channel "My Bus 1 [2]" in the above example) so that it is in the same eye as the other channels. The Suggested Position from Eye Finder (green triangle) will also move to the new eye. Repeat the above step for all remaining stray channels.

9 Select the Run button in the Eye Finder window again.

The following example shows all sampling positions aligned and in the correct eye.



Test Pod 1 in 250 Mb/s Mode

The steps that follow include pass/fail criteria.

Determine PASS/FAIL (1 of 2 tests)

1. PASS/FAIL: If an eye exists near 300 ps for every bit, and Eye Finder places a blue bar in the narrow eye for each bit, then the logic analyzer passes this portion of the test. Record the result in the "Test 1 of 2: Eye Finder locates an eye for each bit" section of the Performance Test Record (page 60).
2. If an eye does not exist near 300 ps for every bit or Eye Finder can not place the blue bar in the narrow eye, then the logic analyzer fails the test. Record the result in the "Test 1 of 2: Eye Finder locates an eye for each bit" section of the Performance Test Record (page 60).

Close the Eye Finder and Analyzer Setup Windows

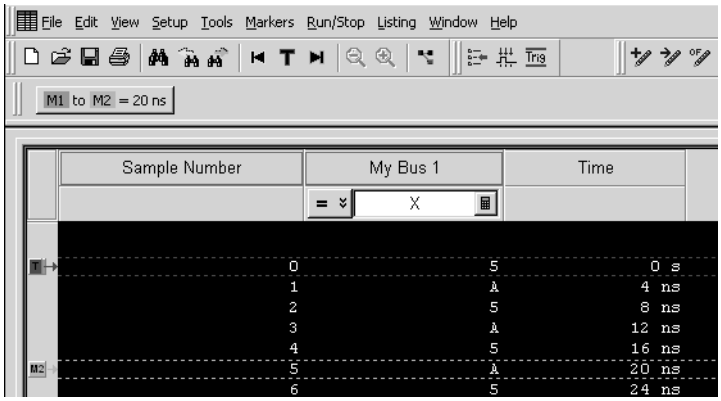
1. Select OK to close the Eye Finder window.
2. Select OK to close the Analyzer Setup window.

Configure the markers

Data must be acquired before the markers can be configured. Therefore, you will need to run the analyzer to acquire data.

1. Switch to the Listing window by selecting the Listing tab at the bottom of the main window.
2. Select the Run icon  .

3 Data will appear in the Listing Window upon completion of the run.

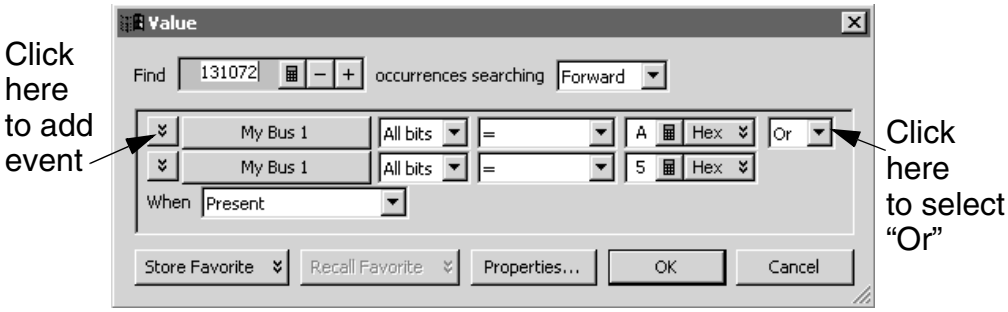


4 From the Main Menu choose Markers→New.

a You can accept the default name for the new marker.

b Change the Position field to Value.

c Select the Occurs... button and create the marker setup shown below.



5 In the Value window, select the Properties... button.

6 In the Value Properties window, select Stop repetitive run when value is not found.

7 Select OK to close the marker Value Properties window.

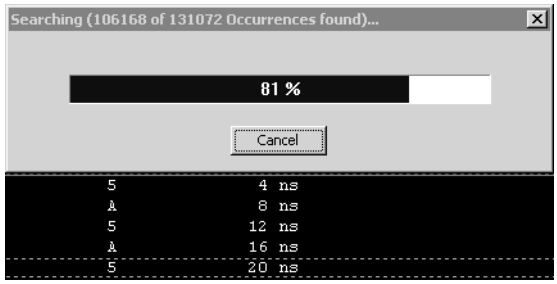
8 Select OK to close the marker Value window. The system will search the display for the occurrences specified.

9 Select OK to close the New Marker window.

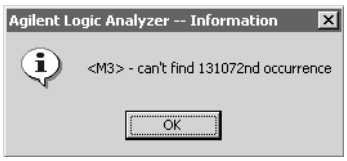
Determine PASS/FAIL (2 of 2 tests)

Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error window will appear.

1 Select the Run Repetitive icon  . Let the logic analyzer run for about one minute. The analyzer will acquire data and the Listing Window will continuously update.



If the "can't find occurrence" window appears, then the logic analyzer fails the test.



Check your test setup. If the failure is not the result of a problem with the test setup, record the failure in the "Test 2 of 2: Correct number of occurrences detected" section of the Performance Test Record (page 60).

NOTE: Be sure that the black ground lead is making good contact with the ground pin on the test connector.

2 When about one minute has elapsed, select the Stop button  to stop the acquisition.

If the "can't find occurrence" window does not appear, then the analyzer passes the test. Record "Pass" in the "Test 2 of 2: Correct number of occurrences detected" section of the Performance Test Record (page 60).

NOTE:

As a point of curiosity, you may want to determine the absolute minimum pulse width and/or absolute maximum frequency at which data can be acquired. The "Performance Test Record" on page 60 does not include places for recording these values because the Performance Verification procedure only verifies that the logic analyzer meets specifications. Determination of additional parameters is not required, but may be performed at the discretion of the calibration laboratory.

On some pulse generators, the signal outputs may become unstable for a short period of time when the signal parameters are adjusted. Adjusting the pulse generator while the logic analyzer is running can cause a false failure.

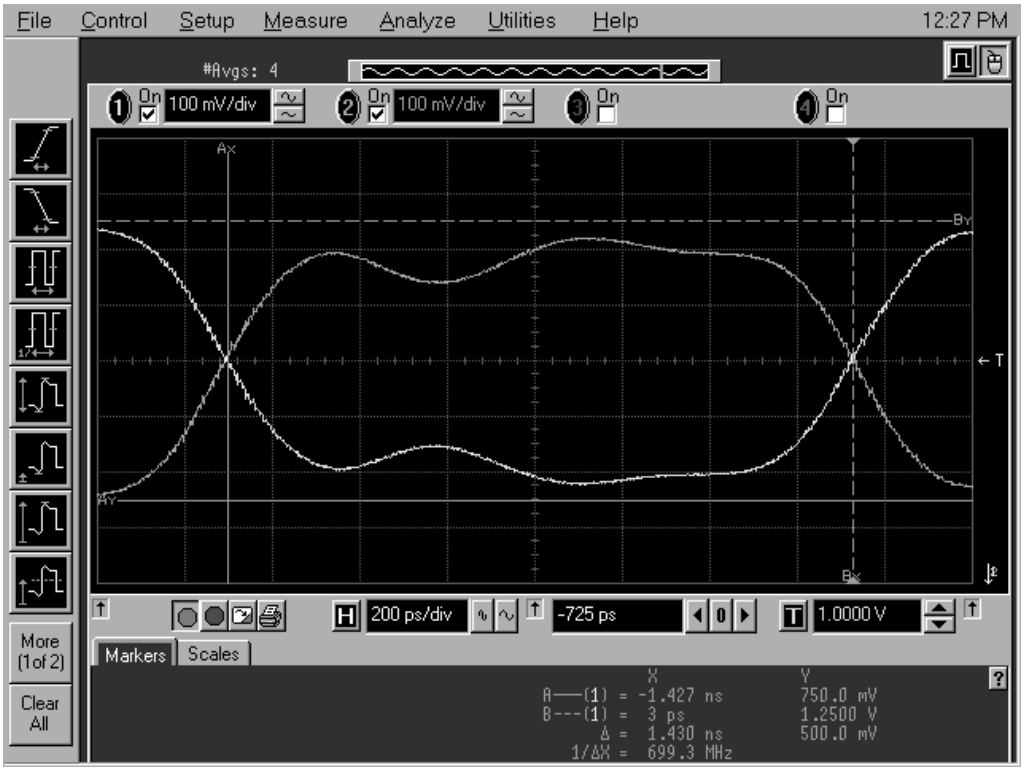
If the error message is displayed immediately after making an adjustment to the pulse generator, select OK to close the error display window and re-run the logic analyzer.

Test the complement of the bits (250 Mb/s mode)

Now test the logic analyzer using complement data.

1. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.
2. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -725 ps (or as required) to center the measured pulse on the oscilloscope display.
3. Verify the DC offset and adjust it if necessary. See page 36.
4. Deskew the oscilloscope if necessary. See page 37.
5. Adjust the oscilloscope's measurement markers to measure the pulse width. Set the markers so that Δ=1.43 ns (this assumes you are using the 8133A pulse generator and the Infiniium 54845A oscilloscope). Adjust the pulse generator so that the pulse width is 1.43 ns as measured by the

markers. See page 39 for details.



6 Adjust the sampling positions using Eye Finder. See page 44.

7 Determine pass or fail (1 of 2 tests). See page 47.

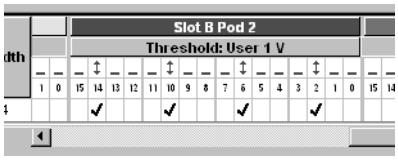
8 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

9 Select the Run Repetitive icon  .

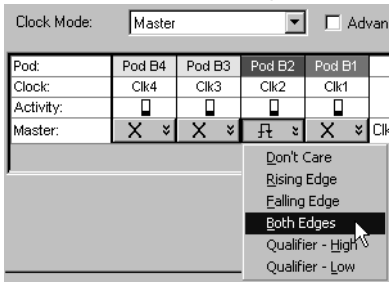
10 Determine pass or fail (2 of 2 tests). See page 49.

Test Pod 2 in 250 Mb/s Mode

1. Disconnect the E5383A Flying Lead Probe Set from Pod 1 and connect it to Pod 2 of the logic analyzer. Do not remove the flying leads that are connected to CLK and the data channels.
2. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.
3. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 725 ps (or as required) to center the measured pulse on the oscilloscope display.
4. Verify the DC offset and adjust it if necessary. See page 36.
5. Deskew the oscilloscope if necessary. See page 37.
6. Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 39.
7. From the Logic Analysis System main menu, select Setup→My 1691xA→Bus/Signal...
8. Scroll to the right and unassign all Pod 1 bits.
9. Ensure that the Pod 2 threshold is set to 1 volt (see page 41).
10. Assign bits 2, 6, 10, and 14 of Pod 2.



11. Select the Sampling tab (at the top of the window). In the State Options area, set clock Clk1 to Don't Care.
12. Set Clk2 to Both Edges.



13 Adjust the sampling positions using Eye Finder. Be sure to expand "My Bus 1" and use the recommended starting position noted on page 44. Realign any stray channels if necessary. See page 46.

14 Determine pass or fail (1 of 2 tests). See page 47.

15 Select OK to close the "Analyzer Setup" window.

16 Switch to the Listing window by selecting the Listing tab at the bottom of the main logic analyzer window.

17 Select the Run Repetitive icon  .

18 Determine pass or fail (2 of 2 tests). See page 49.

Test the complement of the bits (Pod 2, 250 Mb/s mode)

1 Test the complement of the bits. See page 50.

Test the Remaining Pods in 250 Mb/s Mode

1 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate. Test using clock Clk3 for Pod 3, clock Clk4 for Pod 4, etc. Upon completion, the logic analyzer is completely tested in the 250 Mb/s mode. The 16910A has six pods; the 16911A has four pods.

Test Pod 1 in 500 Mb/s Mode

NOTE: If option 500 is not installed on the 16910/11A module, then 250 MHz will be the only speed available. In this case, write "n/a" in the 500Mb/s mode boxes in the Performance Test Record and proceed to "Conclude the State Mode Tests" on page 59.

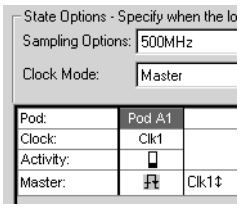
Clock "Clk1" will be used for testing all pods in the 500 Mb/s mode. Therefore two E5383A Flying Lead Probe sets will be required when testing the remaining pods.

You will use a test frequency of 125 MHz (plus test margin) to determine the correct eye in the Eye Finder window. Then you will increase the test frequency to 250 MHz (plus test margin) and perform the test.

1 Disconnect the E5383A Flying Lead Probe from Pod 6 of the 16910A logic analyzer (or from Pod 4 of the 16911A logic analyzer) and connect it to Pod 1 of the logic analyzer.

2 From the Logic Analysis System main menu, select Setup→My 1691xA→Timing/State (Sampling)...

3 In the State Options section, Sampling Options field, select the "500 MHz" mode. The clock mode will change to "Both Edges". No other mode is available.



4 In the logic analyzer's Buses/Signals window, unassign all bits.

5 Assign bits 2, 6, 10, and 14 of Pod 1.

6 Ensure that the Pod 1 threshold is set to 1 volt. See page 41.

Determine and set Eye Finder Position (500 Mb/s mode)

7 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

8 Change the oscilloscope's horizontal position to 725 ps (or as required) to center the measured pulse on the oscilloscope display.

9 Verify the DC offset and adjust it if necessary. See page 36.

10 Verify the oscilloscope Deskew and adjust if necessary. See page 37.

11 Adjust the measured pulse width from the pulse generator to 1.5 ns (minus the test margin) as described on page 39.

Do not change the pulse generator frequency yet.

12 Select the Sampling tab.

13 Select the Sampling Positions button. A dialog will appear telling you that acquired data will be erased. Select the Yes button, erasing acquired data.

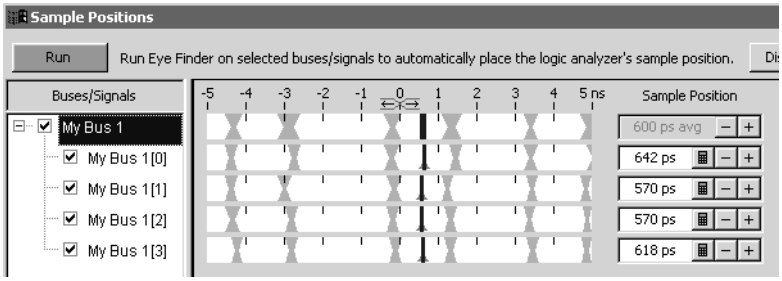
14 In the Eye Finder window, expand "My Bus 1".

15 If the blue bars are not vertically aligned, align them. See page 44.

16 Grab the blue bar for "My Bus 1" and move it to approximately 600 ps. All blue bars will follow.

17 Run Eye Finder and note the average sampling position chosen by Eye Finder:_____ps. In the following example, the average sampling position is 600 ps. Note that in this step, you place the blue bars in the narrow window (not the wide window) that appears just to the right of zero in the Eye Finder display. Then run Eye Finder. The position may be different based on your test setup. Bring stray channels into alignment if necessary.

See page 46.



18 Now set the pulse generator to the new test frequency. The logic analyzer will be tested using a double-edge clock. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 250 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

For example, if you are using an 8133A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 250 MHz plus 2% (255 MHz).

19 The pulse measured on the oscilloscope may have moved slightly. Verify the DC offset and adjust it if necessary. See page 36.

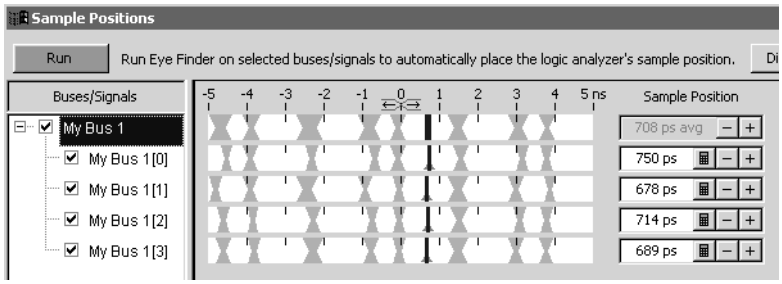
20 Verify the oscilloscope Deskew and adjust if necessary. See page 37.

21 Adjust the measured pulse width from the pulse generator to 1.5 ns (minus the test margin) as described on page 39.

22 Open the Eye Finder window, and align the blue bars vertically. See page 44.

23 Grab the blue bar for “My Bus 1” and move it to the recommended starting position you noted on page 55.

24 Run Eye Finder again. Some eyes may close, but the eyes in the sampling position you chose on page 55 should remain open.



When you close the Analyzer Setup window a dialog may appear. If so, answer

Yes to erase the data and continue.

25 Perform the procedure "Determine PASS/FAIL (1 of 2 tests)" on page 47.

26 Select the Run Repetitive icon  .

27 Perform the procedure "Determine PASS/FAIL (2 of 2 tests)" on page 49.

Test the complement of the bits (Pod 1, 500 Mb/s mode)

Now test the logic analyzer using complement data.

1 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.

2 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -725 ps (or as required) to center the measured pulse on the oscilloscope display.

3 Verify the DC offset and adjust it if necessary. See page 36.

4 Deskew the oscilloscope if necessary. See page 37.

5 Verify that the pulse width is set to 1.5 ns. See page 39.

6 Run Eye Finder and align stray channels if necessary.

7 Perform the procedure "Determine PASS/FAIL (1 of 2 tests)" on page 47.

8 Select the Run Repetitive icon  .

9 Perform the procedure "Determine PASS/FAIL (2 of 2 tests)" on page 49

Test Pod 2 in 500 Mb/s Mode

1 Leave the first E5383A Flying Lead Probe Set connected to Pod 1 of the logic analyzer. Remove the Pod 1 flying leads 2, 6, 10, and 14 from the SMA/Flying Lead test connectors. Do not remove the flying leads that are connected to CLK and $\overline{\text{CLK}}$ flying leads.

2 Connect the second E5383A Flying Lead Probe Set to Pod 2.

3 Connect the Pod 2 E5383A Flying Lead Probe Set's bits 6 and 14 to the

SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 OUTPUT.

4. Connect the Pod 2 E5383A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 $\overline{\text{OUTPUT}}$.
5. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.
6. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.
7. Verify the DC offset and adjust it if necessary. See page 36.
8. Deskew the oscilloscope if necessary. See page 37.
9. Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 39.
10. Unassign all Pod 1 bits.
11. Assign bits 2, 6, 10, and 14 of Pod 2.
12. Ensure that the Pod 2 threshold is set to 1 volt (just as you did for Pod 1 on page 41).
13. Adjust the sampling positions using Eye Finder. Be sure to expand "My Bus 1", align the blue bars vertically, and use the starting position you noted on page 55. Realign any stray channels if necessary. See page 46.
14. Determine pass or fail (1 of 2 tests). See page 47.
15. Switch to the Listing window.
16. Select the Run Repetitive icon  .
17. Determine pass or fail (2 of 2 tests). See page 49.

Test the complement of the bits (Pod 2, 500 Mb/s mode)

1. Test the complement of the bits on Pod 2. You can use the procedure "Test the complement of the bits (250 Mb/s mode)" on page 50 as a guideline.

Test Pods 3 and 4 in 500 Mb/s Mode (16910A only)

1 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate. You must use clock Clk1 on Pod 1 for all tests in the 500 Mb/s mode because the other clocks are not available in this mode. Upon completion, the logic analyzer is completely tested.

2 Complete the Performance Test Record on page 60.

Conclude the State Mode Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a In the Logic Analysis System window, select the [X] in the upper right corner to close the window. At the query “Do you want to save the current configuration?” select No.

Ending and restarting the logic analysis session will re-initialize the system.

b Disconnect all cables and adapters from the pulse generator and the oscilloscope.

Performance Test Record

LOGIC ANALYZER MODEL NO. (circle one): 16910A 16911A

Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Years Recommended next testing:

TEST EQUIPMENT USED

Pulse Generator Model No.	Oscilloscope Model No.
Pulse Generator Serial No.	Oscilloscope Serial No.
Pulse Generator Calibration Due Date:	Oscilloscope Calibration Due Date:

MEASUREMENT UNCERTAINTY

Clock Rate	**Pulse Width (Eye Width)**
Pulse Generator Frequency Accuracy: 8133A: 1% of setting	Oscilloscope Horizontal Accuracy: 54845B: ±[((0.007%) (Δt) + (full scale/(2x memory depth)) + 30 ps] ≅ 30 ps Oscilloscope Display Resolution: 54845B: ± 5 ps
Setting: 125 MHz + 2% = 127.5 MHz 250 MHz + 2% = 255 MHz	Pulse Width setting: 1.43 ns PWmax(worst case) = 1.43 ns + 30 ps + 5 ps = 1.465 ns

TEST RESULTS

Logic Analysis System Self-Tests (Pass/Fail):				
Performance Test: Minimum Master to Master Clock Time and Minimum Pulse Width				
	250 Mb/s mode		**500 Mb/s mode (if option 500 is installed)**	
Pulse Generator Settings	Freq: 125 MHz plus test margin Pulse Width: 1.5 ns less test margin		Freq: 250 MHz plus test margin Pulse Width: 1.5 ns less test margin	
Test Criteria	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail):				
Pod 2 Results (pass/fail):				
Pod 3 Results (pass/fail):				
Pod 4 Results (pass/fail):				
Pod 5 Results (pass/fail):				
Pod 6 Results (pass/fail):				

4

Calibrating

This chapter gives you instructions for calibrating the logic analyzer.

Calibration Strategy

The 16910/11A logic analyzer does not require an operational accuracy calibration. To test the module against the module specifications, refer to the “Testing Logic Analyzer Performance” chapter on page 19.

5

Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies.

The troubleshooting consists of flowcharts, self-test instructions, and a cable test.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

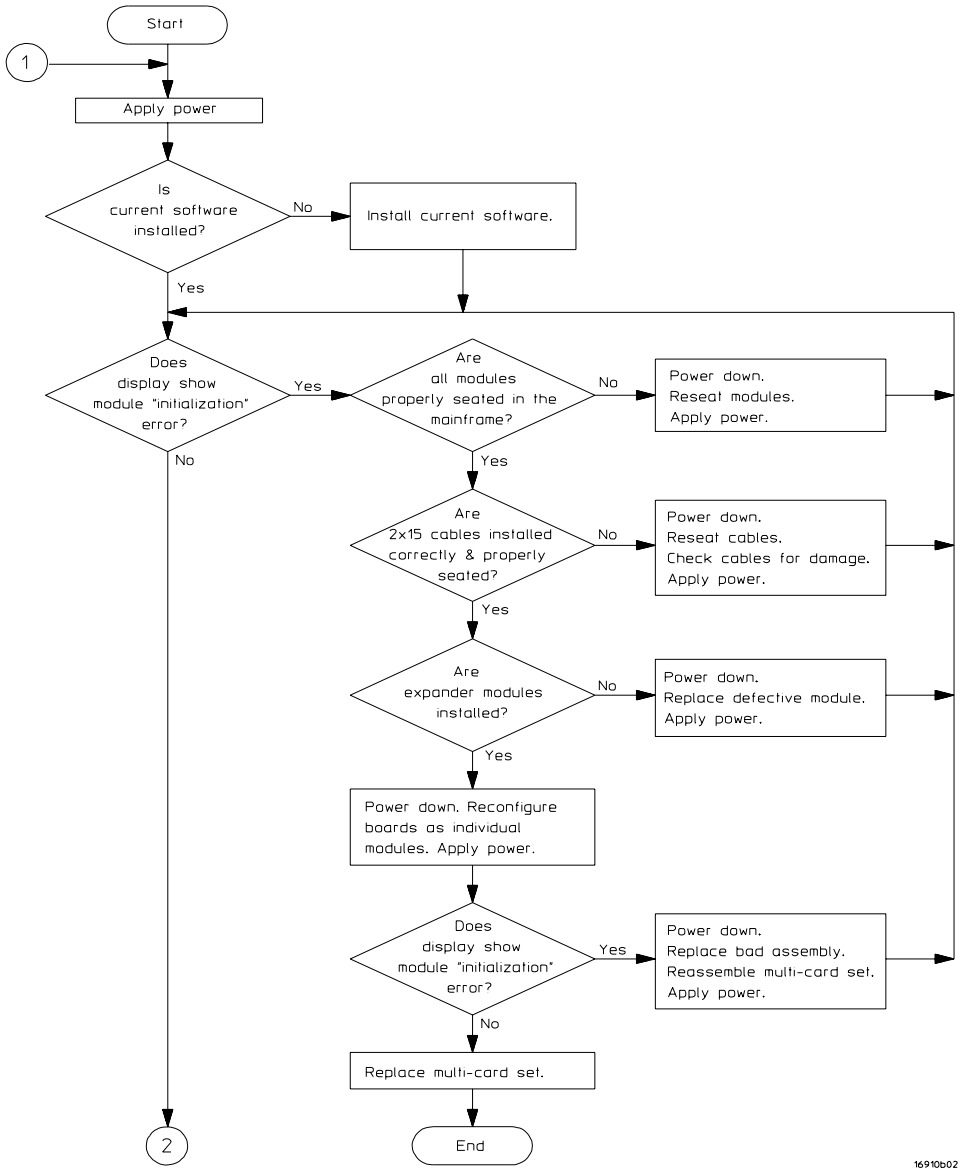
CAUTION: Electrostatic discharge can damage electronic components. Use grounded wrist-straps, mats, and standard ESD precautions when you perform any service to the mainframe or the modules in it.

CAUTION: For protection against electrostatic discharge (ESD), package the module in ESD-safe material when returning it to Agilent Technologies for service.

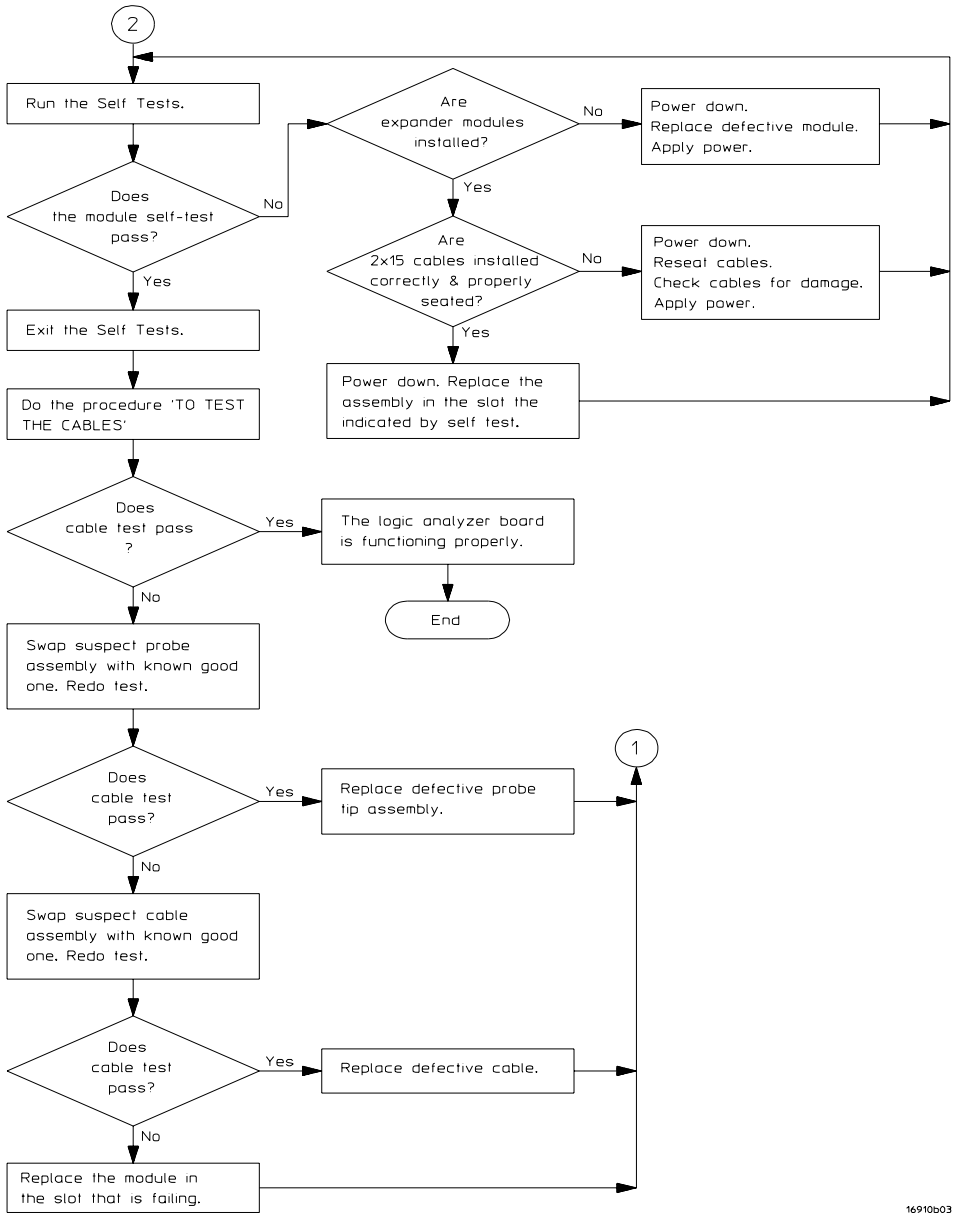
To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

If the module still doesn't work correctly after completing all the procedures described in the flowchart, return it to Agilent Technologies for repair. Be sure to include a note describing the problem in detail.



Troubleshooting Flowchart 1



Troubleshooting Flowchart 2

To run the self tests

1 See “Perform System Self-Tests” on page 30.

Self-Test Descriptions

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

Interface FPGA Register Test. The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. This FPGA must be working before any of the other circuits on the board will work. The backplane FPGA is the interface between the backplane and the Memory Controller FPGAs and Analysis Chips. Also, the Backplane FPGA generates the board ID code that is used to identify the module and slot.

Load Memory FPGA Test. The purpose of this test is to verify that the Memory Controller FPGAs can be loaded with their respective configuration data files.

Memory FPGA Register Test. The purpose of this test is to verify that the registers in the Memory Controller FPGAs can be written to and read back.

EEPROM Test. The purpose of this test is to verify:
The address and data paths to the EEPROM
That each cell in the EEPROM can be programmed high and low
That individual locations can be independently addressed
The EEPROM can be block erased

Memory Data Bus Test. The purpose of this test is to check the data write/read access of the acquisition RAM from the module backplane bus. This test verifies the operation of the RAM data bus as well as some of the operation of the RAM control and address busses. This is the first test that accesses the RAM acquisition memory using the Memory Controller FPGAs.

Memory Address Bus Test. The purpose of this test is to completely verify the acquisition RAM address lines.

Memory Signals Test. The purpose of this test is to verify signal integrity and proper read/write synchronization between the Memory Controller FPGAs and the acquisition RAM memory devices.

HW Assisted Memory Cell Test. The purpose of this test is to fully check all of the addresses in all acquisition RAM memory devices.

Memory Unload Modes Test. The purpose of this test is to check the various

modes of unloading data from the acquisition RAM devices. These modes are setup by writing to registers in the Memory Controller FPGAs. These FPGAs sequence the data and perform data decoding based on the mode.

DMA Test. The purpose of this test is to check the various modes of unloading data from the acquisition RAM memories using DMA backplane transfers. This test is essentially the same as the Memory Unload Modes Test except that DMA backplane transfers are used to read the data from the board.

HW Accelerated Search Test. This test verifies the Memory Controller FPGA-based HW Accelerated Search function.

Chip Registers Read/Write Test. The purpose of this test is to verify that each writable bit in each register of the Analysis chips can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

LA Chip Calibrations Test. The purpose of this test is to verify that each analysis chip in the module is able to successfully complete self-calibration.

Analyzer Chip Memory Bus Test. The purpose of this test is to check the Analysis chip memory busses that go between the Analysis chips and the Memory Controller FPGAs.

System Clocks Test. The purpose of this test is to verify that the four clocks (1/2/3/4) are functional between the master board and all Analysis chips, and that the two Psync lines (A/B) are functional between the master board's Analysis chips and all Analysis chips in the module. This test verifies that the four clock lines are driven from the master board and can be received by all Analysis chips, and that the Psync lines can be driven by each master chip on the master board and received by all other Analysis chips in the module.

Turbo Clock Divider Test. The logic analyzer has a clock divider on the board, used for single edge turbo state. This test verifies that the divider routing works, and that it resets low.

System Backplane Clock Test. The purpose of this test is to verify the system backplane 100 MHz clock is functional to each Analysis chip and running at the correct frequency. This test also verifies that the PLL in each chip can be configured in bypass mode (PLL is not used), then verifies that the PLL can be enabled and used to generate additional clock frequencies.

Comparators Test. The purpose of this test is to verify that the front-end signal comparators are able to be set to maximum and minimum thresholds and that they are able to recognize activity on each input using the cal input clock.

Inter-chip Resource Bus Test. The purpose of this test is to verify that the Inter-chip Resource lines (ICRs) can be driven as outputs and received as inputs

by each chip in the module.

Inter-module Flag Bits Test. The purpose of this test is to verify that the 4 Inter-module Flag Bit Output lines can be driven out from the master chip in the module and received by each chip in the module.

Global and Local Arm Lines Test. The purpose of this test is to verify that each Analysis chip on the master board can receive the Local Arm signal, and the Global Arm signal can be driven by the bottom and top chips on the master board and received by all chips in the module (master and slave). Note that the middle analysis chip cannot drive the Global Arm signal (left unconnected).

Timing Zoom Memory BIST Test. This test verifies that the timing zoom SRAM embedded in the analysis chips is functional.

Timing Zoom Memory Addr/Data Test. This test verifies connectivity of components within the analysis chip. It verifies that the address, data, and clock lines of the timing zoom circuitry is correct.

To exit the test system

1 Simply close the self-test window. No additional actions are required.

To Assemble the 2 x 9 Test Connectors

The 2 x 9 test connectors are used to connect all 16 channels and the clock of the logic analyzer to the pulse generator so you can test the flying lead probe and cables. (See "To test the cables" on page 73.)

Materials Required

Material	Critical Specification	Recommended Model/Part
Pin Strip Header (Qty 1, which will be separated)	.100" x .100" Pin Strip Header, straight, pin length .230", two rows, .120" solder tails, 2 x 40 contacts	3M 2380-6121TN or similar 2- row with 0.1" pin spacing
Jumper wire	< 6 inches, approximately 22 gauge	
Resistor, 100 ohm 1% (Qty 4)		
SMA Board Mount Connector (Qty 2)		Johnson 142-0701-801 (see www.johnsoncomponents.com)

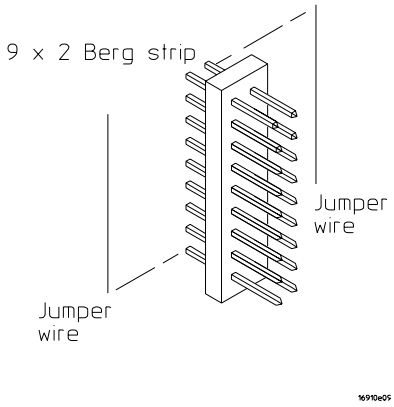
Build two test connectors using SMA connectors and 2-by-9 sections of pin strip.

1 Prepare the pin strip header:

a Cut or cleanly break two 2 x 9 sections from the pin strip.

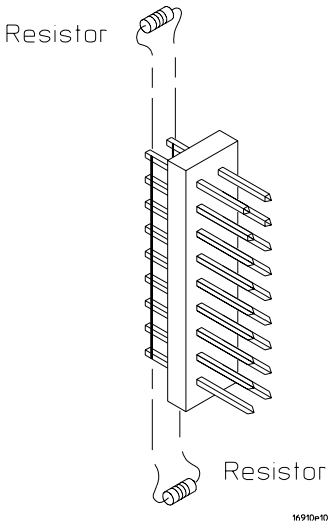
b Solder a jumper wire to all nine pins on one side of the pin strip.

c Solder a jumper wire to all nine pins on the other side of the pin strip.



d Solder two resistors to the pin strip, one at each end between the end

pins.

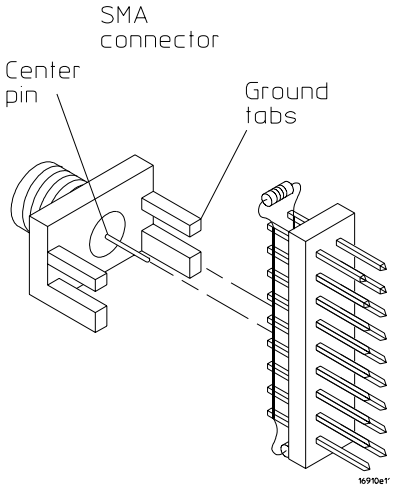


e Repeat for the second 2 x 9 pin strip.

2 Attach the SMA connector:

a Solder the center pin of the SMA connector to the center pin of one row on the pin strip.

b Solder the ground tab of the SMA connector to the pins of the other row on the pin strip.



c Repeat for the second 2 x 9 pin strip.

3 Check your work and de-flux the assembies if desired.

To test the cables

This test allows you to functionally verify the logic analyzer cable and the flying lead probe of any of the logic analyzer pods. Only one probe and cable can be tested at a time. Repeat this test for each probe and cable to be tested. Two Flying Lead Probes are required if you need to test pods other than Pod 1 because the clock from Pod 1 will be used to acquire data.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	40 MHz, 3 ns pulse width, < 600 ps rise time	8133A Option 003
2 x 9 Test Connectors (Qty 2)	no substitute	See "To Assemble the 2 x 9 Test Connectors" on page 71.
SMA m-m adapter (Qty 2)		Johnson 142-0901-811 SMA Plug to Plug or similar
Flying Lead Probe (Qty 2)	no substitute	HP or Agilent E5383A

Set up the test equipment

1 If you have not already done so, do the procedure "Perform System Self-Tests" on page 30.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table:

Pulse Generator Setup

Timebase	Pulse Channel 2	Trigger	Pulse Channel 1
Mode: Int Freq: 40 MHz	Mode: Pulse ÷ 1 Delay: (not available in pulse mode) Width: 3 ns Ampl: 3 V Offs: 1.5 V Output: Enable (LED off) Comp: Normal (LED off) Limit: Off (LED off) $\overline{\text{Output}}$: Enable (LED off)	Disable (LED on)	Doesn't matter, not used in this test.

Connect the test equipment

1 Using two 2 x 9 test connectors, connect the logic analyzer to the pulse generator channel outputs.

   a Connect the even-numbered channels to the pulse generator Channel 2 OUTPUT.

   b Connect the odd-numbered channels the pulse generator Channel 2 $\overline{\text{OUTPUT}}$.

2 Connect Clk1 to the pulse generator Channel 2 OUTPUT.

3 Enable the pulse generator Channel 1 and Channel 2 outputs (LEDs off).

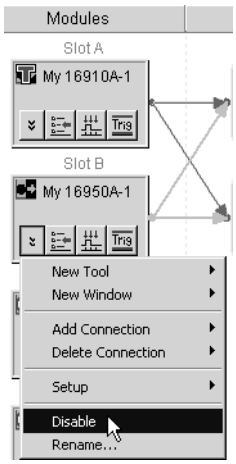
Configure the logic analyzer to test Pod 1

1 Exit the logic analysis application (from the main menu, choose File→Exit) and then restart the application. This puts the logic analysis system into its initial state.

2 Disable all logic analyzers other than the analyzer under test.

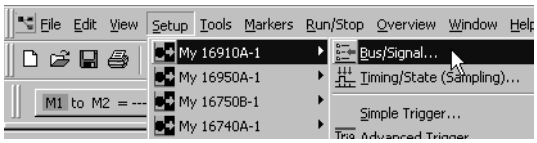
   a Select the Overview tab at the bottom of the main window.

   b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.

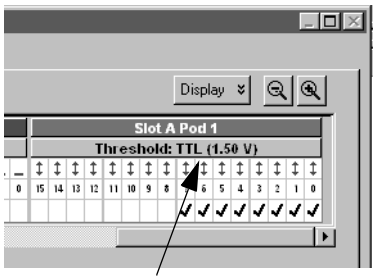


3 Set up the bus and signals to test Pod 1.

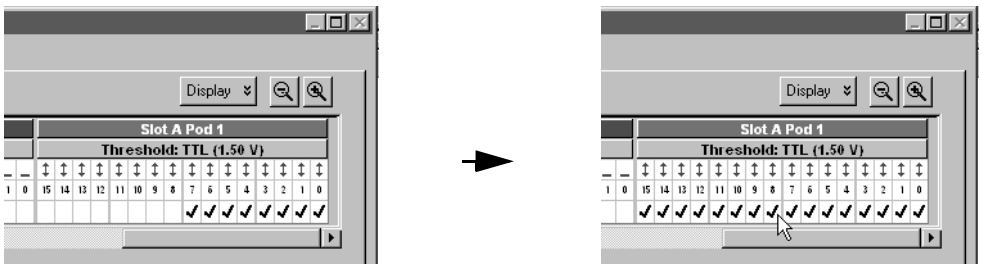
a From the Logic Analysis System main menu, select Setup→My 1691xA→Bus/Signal....



b In the Analyzer Setup window, ensure that the Threshold button for Pod 1 is set to TTL (1.50 V).



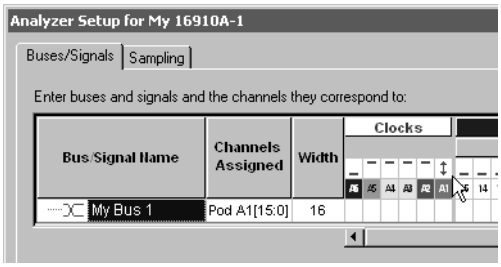
c Verify that the activity indicators (the red arrows) show activity on all 16 channels that are connected to the pulse generator.



d Assign all channels. Hint: you can do this quickly by clicking on the left-most channel, then dragging to the right across all of the other channels. If you have a model 16902A logic analysis system mainframe you can touch the touchscreen and drag across with your finger.

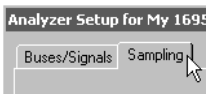
e Drag the scroll bar all the way to the left and ensure that the activity

indicator shows activity on clock 1.

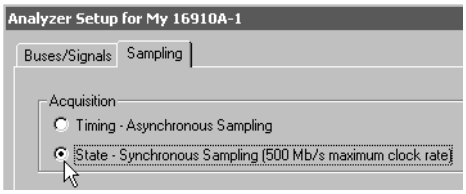


4 Set the sampling mode.

a Select the Sampling tab of the Analyzer Setup window.

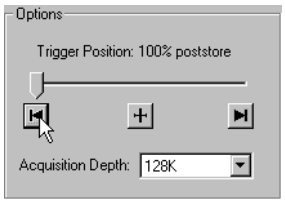


b Select State Mode.

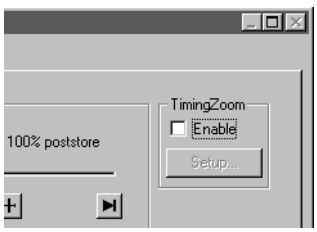


c Set the Trigger Position to 100% Poststore.

d Set the Acquisition Depth to 128K.



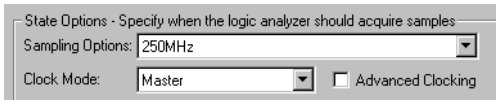
e Clear the Timing Zoom check box to turn Timing Zoom off.



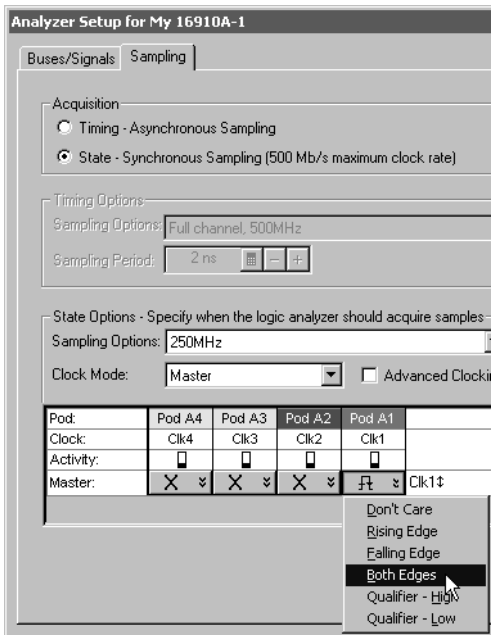
f Ensure that the sampling speed is set to 250 MHz in the Sampling Options box.

NOTE: If option 500 is not installed on the 16910/11A module, then 250 MHz will be the only speed available.

g Ensure that the Clock Mode is set to Master.

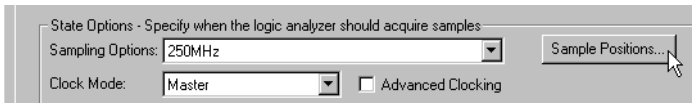


h Set the clock mode to Both Edges.

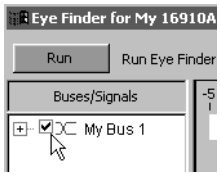


Adjust sampling positions using Eye Finder

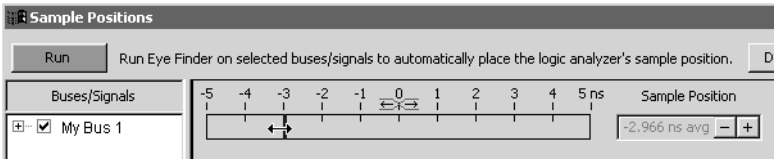
1 Select the Sample Positions button. The Eye Finder window will appear.



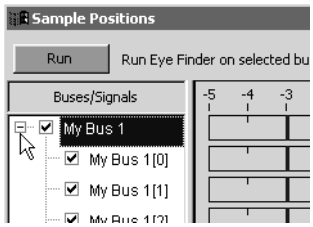
2 In the "Buses/Signals" section of the Eye Finder window, ensure that the check box next to "My Bus 1" is checked.



3 Drag the blue bar for "My Bus 1" to approximately -3 ns.



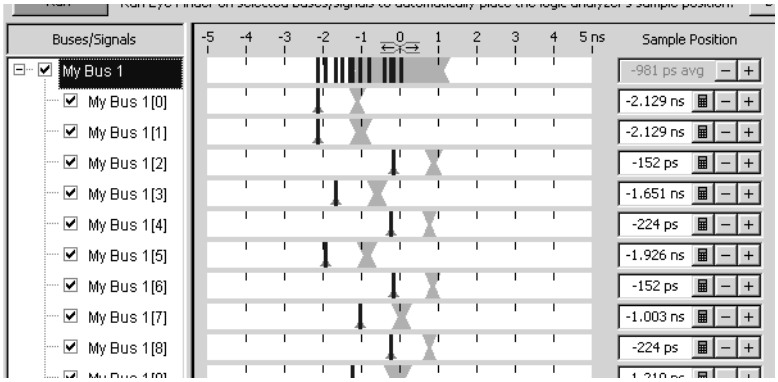
4 Select the plus sign to expand bus "My Bus 1".



5 Select the Run button in the Eye Finder window.

6 Ensure that an eye appears for each bit. Depending on your test setup, the eye position may vary. Ensure that all blue bars in the individual channel rows (excluding the top row) are to the left of the orange transition

region. If not, see "To re-align a stray channel" on page 46.



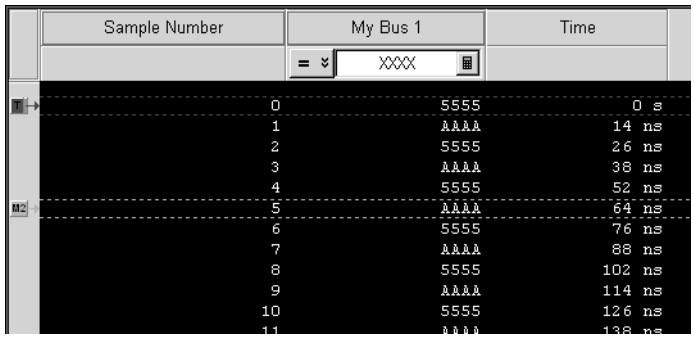
7 Select OK to close the Sample Positions window.

8 Select OK to close the Analyzer Setup window.

9 Switch to the Listing window by selecting the Listing tab at the bottom of the main window.

10 Select the Run icon  .

11 Data will appear in the Listing Window upon completion of the run.



12 If the listing shows that the data alternates between AAAA and 5555, then the probe and cable pass the test.

If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- open channel.
- channel shorted to a neighboring channel.
- channel shorted to either ground or a supply voltage.

Connect and configure the logic analyzer to test other pods

1 Disconnect all flying lead probes from the 2 x 9 test fixtures.

2 Connect the second E5383A Flying Lead Probe set to the next pod to be tested.

NOTE: In this example the pod to be tested will be Pod 2.

3 Connect the even bits of Pod 2 to the 2 x 9 test fixture at the pulse generator's OUTPUT 2.

4 Connect the odd bits of Pod 2 to the 2 x 9 test fixture at the pulse generator's $\overline{\text{OUTPUT 2}}$.

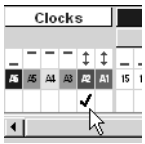
5 If the pod to be tested (Pod 2 in this example) has a clock bit, connect it to the 2 x 9 test fixture at the pulse generator's OUTPUT 2.

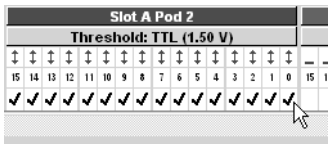
NOTE: Pods 5 and 6 of the 16910A logic analyzer do not have clock bits. All others do.

6 Connect the clock bit from Pod 1 to the 2 x 9 test fixture at the pulse generator's $\overline{\text{OUTPUT 2}}$.

7 In the Analyzer Setup window, Buses/Signals tab, un-assign all channels of Pod 1.

8 Assign all channels of the pod to be tested. If the pod to be tested has a clock, then assign it too (place a check mark in the box under the channel name).

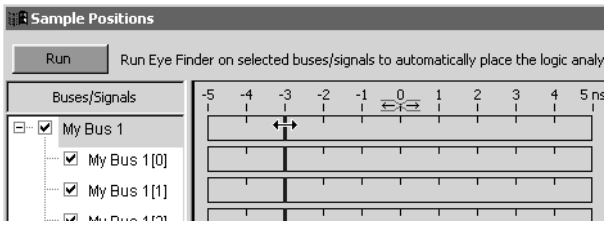




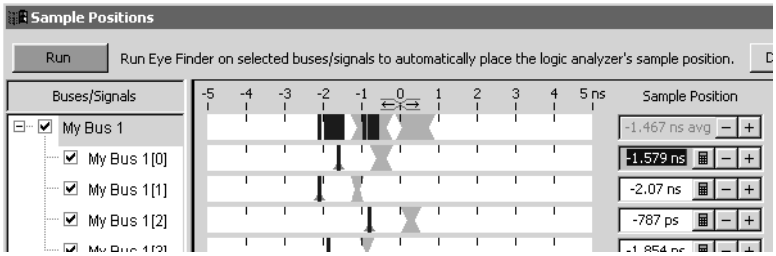
9 Select the Sampling tab.

10 Select the Sampling Positions button.

11 Move the starting position to -3 ns.



12 Run Eye Finder and ensure that an eye is found for each bit.

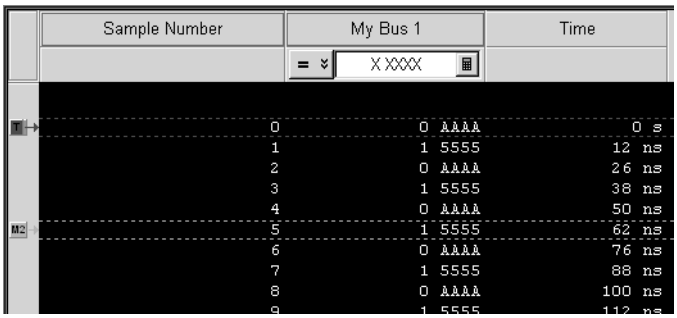


13 Select OK to close the Eye Finder window.

14 Select OK to close the Analyzer Setup window.

15 Switch to the Listing window and run the logic analyzer.

16 Examine the listing. If the listing shows that the data alternates between 0 AAAA and 1 5555 (or AAAA and 5555 if the pod does not have a clock bit), then the probe and cable pass the test.



If the listing does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include:

- open channel.
- channel shorted to a neighboring channel.
- channel shorted to either ground or a supply voltage.

17 Perform the test on all remaining pods, always using CLK 1 to clock in the data.

18 Return to the troubleshooting flow chart.

6

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module as well as the instructions for returning assemblies.

CAUTION: Turn off the mainframe before installing, removing, or replacing a module.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wrist-straps, mats, and standard ESD precautions when you perform any service to the mainframe or the modules in it.

Tools Required

- A T10 TORX screwdriver is required to remove screws that hold the probe cables to the back panel.

To remove the module

Instructions for removing or installing the module into the mainframe can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16900A-series mainframe, go to www.agilent.com and enter **16900A installation guide** in the quick search box. Then scroll down to **Manuals, Guides & Notifications** to find the *16900A-Series Logic Analysis Systems Installation Guide*.

To remove the logic analyzer cable

1. Remove power from the instrument
   - **a** In the session manager, select Shutdown.
   - **b** At the query, select Power Down.
   - **c** When the "OK to power down" message appears, turn the instrument off.
   - **d** Disconnect the power cord.
2. Remove the logic analyzer cable.
   - **a** Use a T10 Torx driver to remove the screws that secure the logic analyzer cable to the rear panel.
   - **b** Gently lift the logic analyzer cable end connector from the circuit board connector.
3. If the logic analyzer cable is faulty, replace the cable and follow the next procedure to install the replacement logic analyzer cable.

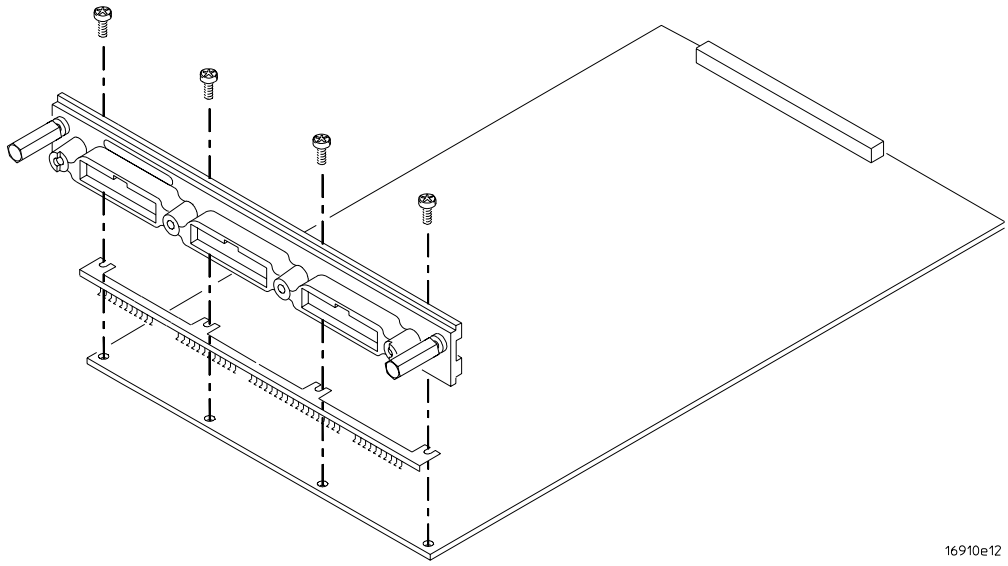
To install the logic analyzer cable

1. Connect the logic analyzer cable to the logic analyzer circuit board.
   a. Align the logic analyzer cable end connector with the circuit board cable connector and gently apply pressure to seat the logic analyzer cable onto the circuit board connector.
2. Secure the cable to the rear panel.
   a. Install the T10 screws (two per cable) and tighten to 5 in/lb.

CAUTION: If you over tighten the screws, damage to the rear panel may occur. Tighten the screws only enough to hold the cable in place, approximately 5 in/lb.

To replace the circuit board

1. Remove the logic analyzer cables using the "To remove the logic analyzer cable" procedure on page 85.
2. Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.
3. Replace the faulty circuit board with a new circuit board. On the faulty board, make sure the 2x15 (30-pin) ribbon cable is connected between J15 and J12.
4. Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.
5. Install the logic analyzer cables using the procedure "To install the logic analyzer cable" on page 86.



To return assemblies

Before shipping the module to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details. Information on contacting Agilent can be found at http://www.agilent.com.

1 Write the following information on a tag and attach it to the module.

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 Remove accessories from the module.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the module.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION: For protection against electrostatic discharge (ESD), package the module in ESD-safe material.

4 Seal the shipping container securely, and mark it FRAGILE.

7

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your module.

Ordering Replaceable Parts

To order a part, visit us on the web at www.parts.agilent.com or call us in the United States at 1-877-447-7278. Or you can contact your nearest Agilent Technologies Sales Office for assistance.

Exchange assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also

"To return assemblies" on page 88.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator (if applicable)
- Agilent Technologies part number
- Total quantity included with the module (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- H Hardware
- J Connector
- MP Mechanical Part
- W Cable

Replaceable Parts

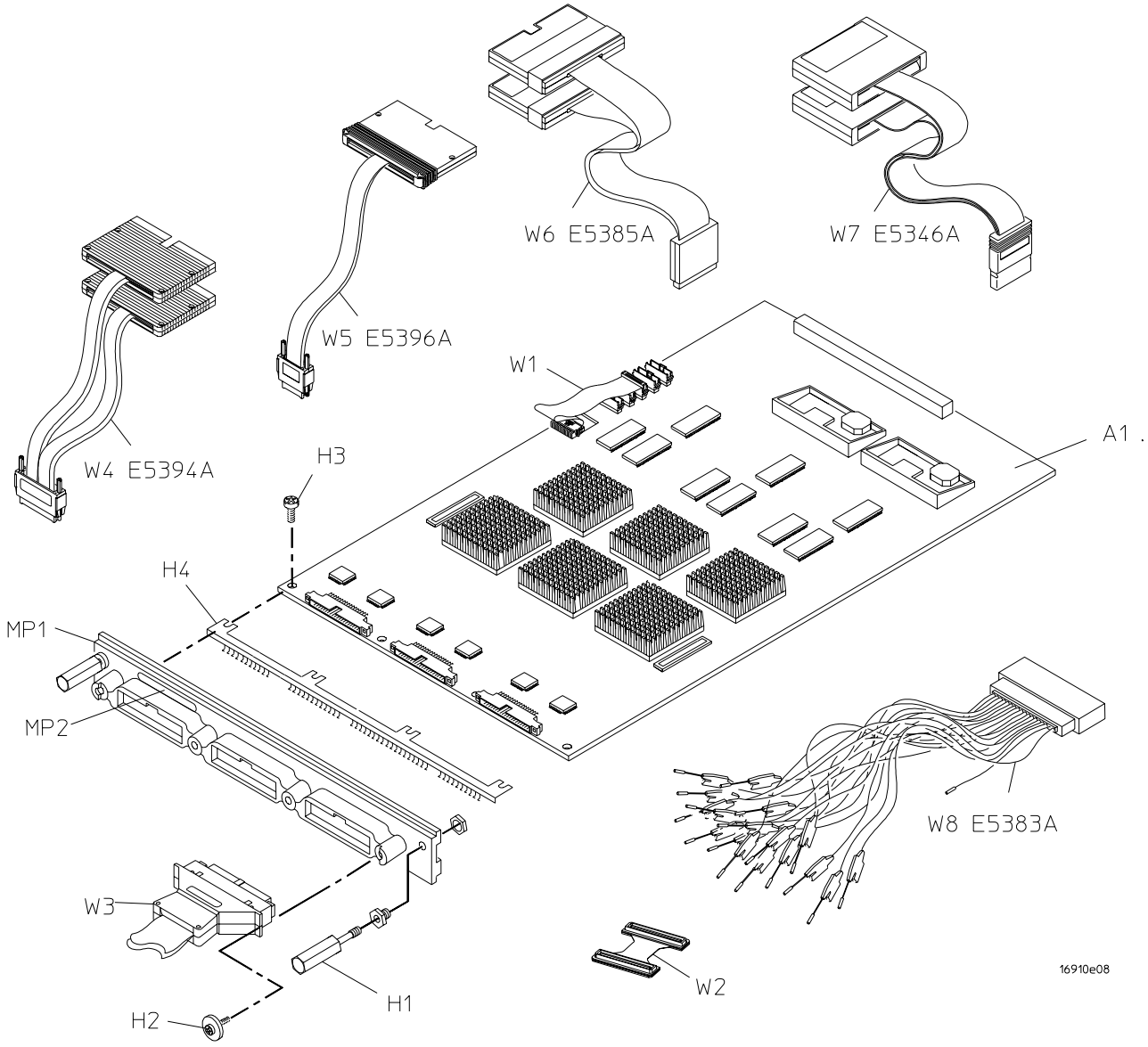
Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assemblies			
	16910-69501		Exchange Acquisition Board Assembly
Replacement Assemblies			
A1	16910-66501	1	Acquisition Board Assembly
H1	16903-68713	2	Replacement Thumb Screws with Sleeve, 2 sets
H1	16900-68713	2	Replacement Thumb Screws with Sleeve, 6 sets
H2	0515-2306	4	MSPH M3.0 x 0.5 10 mm T10 (Cable to Rear Panel)
H3	0515-0430	3	MSPH M3.0 x 0.50 6 mm T10 (Rear Panel to Acquisition Board)
H4	16715-29101	1	Ground Spring
	01650-94312	1	Label - Probe and Cable (Colored labels for identifying probes and cable ends (pods))
MP1	16910-40201	1	Rear Panel
MP2	16910-94301	1	ID Label (16910 only)
MP2	16911-94301	1	ID Label (16911 only)
MP3	16910-04101	1	Cover Plate for Rear Panel (16911 only)
W1	16754-61602	1	2 x 15 Cable
W2	16754-60002	1	2 x 50 Master/Expander Cable Kit (2 pieces)
W3	16715-61601	3 (16910) 2 (16911)	Logic Analyzer Cable

Replaceable Parts

Ref. Des.	Agilent Part Number	Qty	Description
Accessories for Connectivity to the System Under Test			
W8	E5383A		Single-Ended Flying Lead Probe
W5	E5396A		17-pin (half-size) Single-Ended Soft Touch Probe
W4	E5394A		34-Pin Single-Ended Soft Touch Probe
W6	E5385A		100-Pin Single-Ended Probe (for Samtec connector)
W7	E5346A		38-Pin Single-Ended Probe (for MICTOR connector)
	E5339A		Single-Ended Low Voltage Probe (MICTOR)
	E5351A		Single-Ended Probe, No Isolation Networks (MICTOR)
	1253-3620		Samtec Connector
	16760-02302		Shroud for 0.062" PC Boards
	16760-02303		Shroud for 0.120" PC Boards
	16760-68702		*Shroud/Connector Kit for 0.062" PC Boards
	16760-68703		*Shroud/Connector Kit for 0.120" PC Boards
	1252-7431		MICTOR Connector
	E5346-44703		MICTOR Shroud for 0.170" PC Boards
	E5346-44704		MICTOR Shroud for 0.125" PC Boards
	E5346-68700		*Shroud/Connector Kit for 0.125" PC Boards

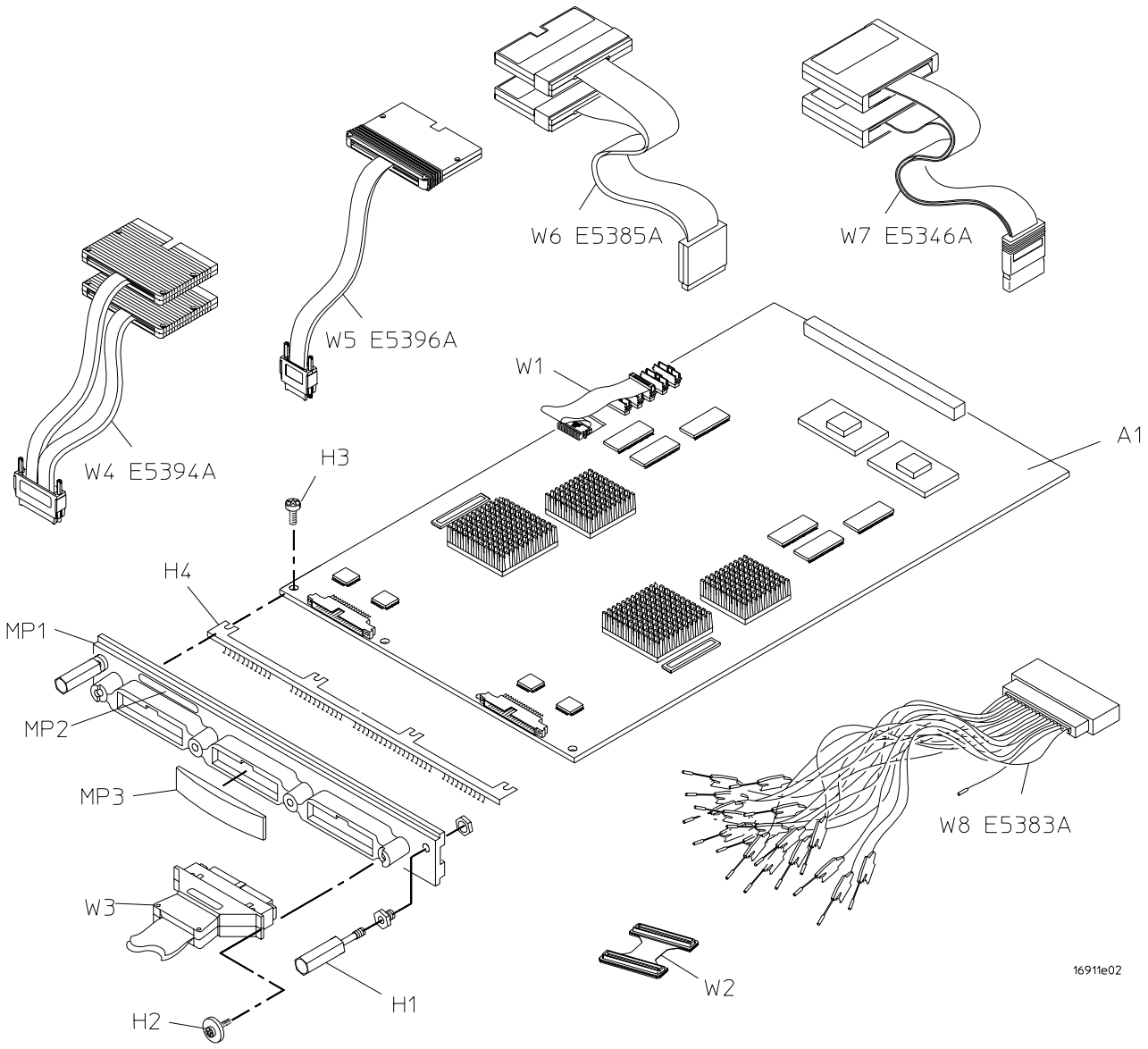
*Shroud/Connector kits include connectors (Qty 5) and shrouds (Qty 5) for the indicated system under test circuit board thickness.

16910A Exploded View



Exploded view of the 16910A logic analyzer

16911A Exploded View



Exploded view of the 16911A logic analyzer

8

Theory of Operation

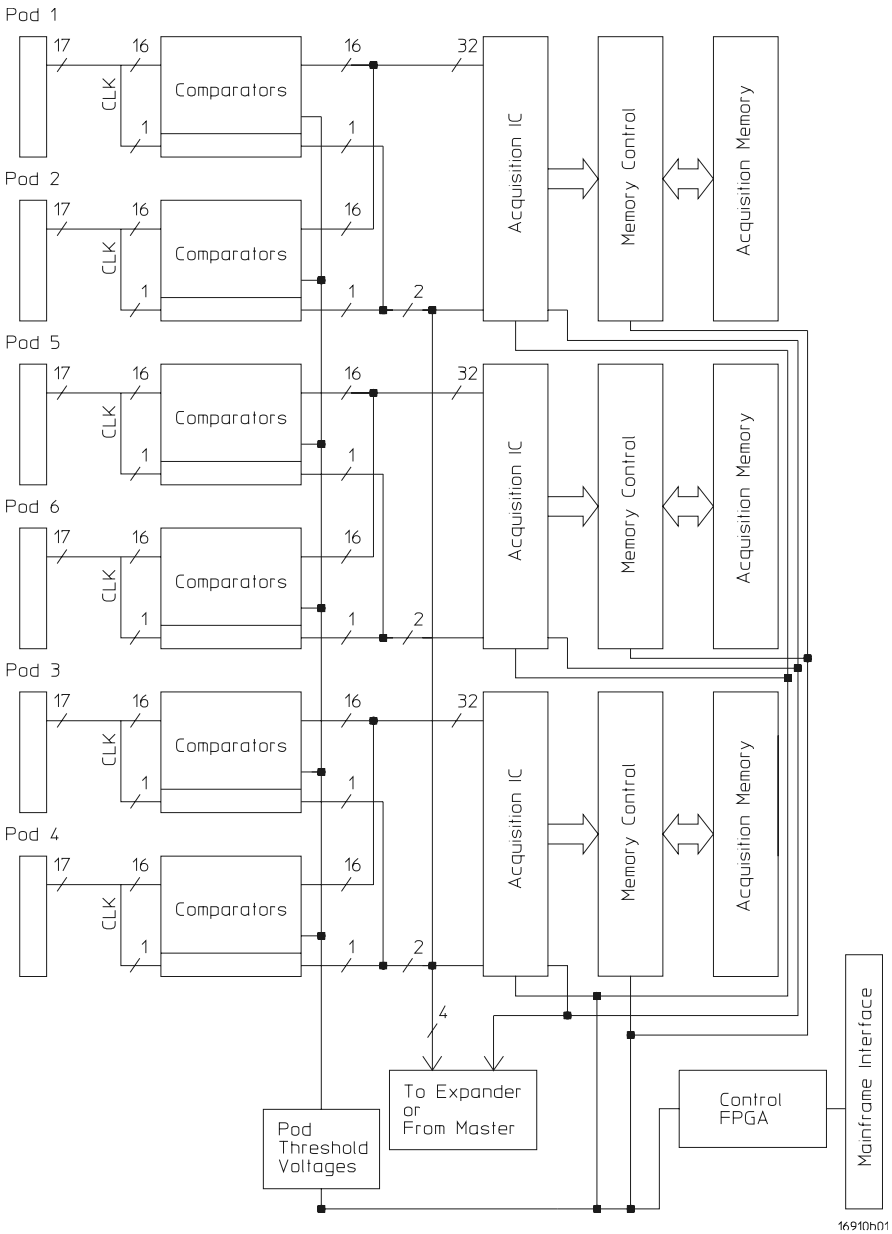
This chapter presents the theory of operation for the logic analyzer card.

The information in this chapter is to help you understand how the logic analyzer operates. This information is not intended for component-level repair.

Block-Level Theory

The block diagram of the 16910/11A logic analyzer is shown below.

The 16910/11A logic analyzer



Probes. The 16910A logic analyzer card contains 6 probe pods; the 16911A contains 4 probe pods. Each pod is comprised of one cable and contains 16 single-ended data channels, a clock channel, two serial I2C programming lines for configuring analysis probes, +5 V for powering analysis probes, and 22 ground signals. Each cable has a 40-pin probe cable connector.

The pods provide +5 Vdc ±5% auxiliary power to each 40-pin probe cable connector. Each connector can deliver up to 300 mA with a maximum of 1.0 A total from the analyzer card. A current limiting circuit protects the +5 V cable power from current overload. The VCC_Enable signal is used to control power to an analysis probe. Currently, the +5 Vdc is only disabled during the I2C self-test.

A variety of single-ended probes can be connected to the logic analyzer cables.

Comparators. The comparators are single-ended devices that interpret incoming data and clock signals as either high or low. A threshold voltage provided by a digital-to-analog-converter (DAC) is coupled to the reference input of the comparator through a precision resistor. Pod thresholds are individually adjustable; clock and data share the same threshold. The comparator outputs drive the acquisition ICs and clock divider circuitry.

Acquisition IC. Each Acquisition IC processes 32 channels of data and 2 channels of clock information. The Acquisition ICs perform data sampling, sequencing, store qualification, pattern recognition, and counting functions. State or Timing sample clocks are sent from the Master card to the Acquisition ICs in each of the Expander cards in a multi-card module. Sampled data is decelerated and passed to the Memory Controller for storage in the Acquisition Memory RAM array.

The Acquisition ICs also contain the 4 GHz sample Timing Zoom circuitry and memory.

Memory Controller and Acquisition Memory. The Memory Controllers store data from the Acquisition ICs into the Acquisition Memory array which is composed of 256 Mbit DDR DRAMs. They also unload data from the memory array after an acquisition is complete, and they deliver the data to the mainframe display system through the mainframe interface connector. In addition they control refresh of the RAM array and can perform a search of stored data.

Master/Expander Connectors. Connectors J9 through J13 and J15 route state and timing clocks, calibration signals, data search signals, and control from the Master card to all cards in the module.

Connectors J20 through J23 route pattern recognition signals between all cards in a card set as well as control clocks from the Master card to other cards in the set.

Mainframe Interface and Control FPGA. The Mainframe interface consists of an FPGA and the Mainframe Interface Connector. The connector brings power

onto the card and provides for control of the card by the analyzer mainframe. It also provides a path for unloading acquired data to the analyzer display.

The FPGA converts bus signals generated by the mainframe processor into control signals for the logic analyzer card. It also provides centralized functions for the card such as I2C, Calibration signals, Flag routing, and Timing mode sample clock.

Index

Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

• Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

• Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

• If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

• Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

• Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

• Do not install substitute parts or perform any unauthorized modification to the instrument.

• Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

• Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

• Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

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Notices

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.